Design and Implementation of a High Speed Residue Number System Correlator for Ultrasonic Time Domain Blood Flow Measurement

Dept. of Electrical and Computer Engineering and
The Coordinated Science Laboratory
University of Illinois, Urbana, IL

ABSTRACT
The design and operation of a high speed residue number system (RNS) digital correlator is presented for implementing the correlation function in a real-time ultrasonic blood flow measurement system. This architecture allows for both high speed processing and a modular design that facilitates construction and testing. This paper discusses the architectural design of the RNS correlator and describes an experimental wire-wrapped prototype that has been constructed for real-time laboratory verification.

1. Introduction
Recently, a new technique of blood flow measurement utilizing ultrasonic time domain correlation in place of the traditional Doppler method was reported [1,2]. The time domain blood flow measurement technique works by analyzing the echoes from a series of ultrasonic pulses. It has been shown in earlier work that particular blood cells scatter ultrasonic energy in a consistent manner over short periods of time. Thus, a particular group of blood cells should return a similar scatter characteristic in every echo in which that group is present in the cone of the ultrasonic pulse. However, because the blood cells are moving within the blood vessel, the characteristic scatter from that group of cells will be spatially displaced in each subsequent echo. By finding the correlation function between adjacent echoes, a time shift can be determined from which scatterer velocity can be calculated.

In order to determine the scatterer characteristic displacement between two echoes, one echo is shifted with respect to the other until the scatterer characteristics are directly superimposed. At this point, the correlation function of the two echoes is maximized. This fact makes it possible to determine when two scatterer characteristics are superimposed and what the shift is between them. Because the temporal spacing of the pulses is known, the velocity of the scatterer can be calculated once the shift has been determined.

Since blood flow velocity is not linear across the width of a blood vessel (it is parabolic, fastest in the center), it is necessary to divide the echo into distinct ranges. Each range is correlated separately with the same range from other echoes to determine a flow velocity in that particular range. A one dimensional (1-D) scan across a blood vessel can be produced by calculating the blood flow velocities for every range within the echo. In addition, a two dimensional (2-D) scan can be produced by taking several 1-D scans at varying angles across the blood vessel. In this manner, a complete image of the flow profile can be produced from which volumetric flow can also be calculated. In [3] the design of a high speed digital correlator based on residue number system (RNS) arithmetic was described. This paper presents the results of an experimental hardware prototype that was constructed according to that design. Ultimately it is hoped that the design presented here will be fabricated as a VLSI monolithic circuit. Some changes required in the current design to facilitate a VLSI implementation are described in Section 5.

2. RNS Correlator Architecture
The purpose of the hardware is to perform a correlation function using the samples from two different echos.

\[ f(a,b) = \sum \chi(a+i) \times \chi(b+i) \]  

In (1), \( x \) and \( \chi \) each represent echos while \( a \) and \( b \) represent the initial offsets into the respective echos. Each echo is composed of 1024 8-bit samples divided into 25 forty-sample ranges which represent different depths across the blood vessel. The samples from a particular range are correlated across different echos to derive a flow rate for that range.

The maximum word length required to calculate a value from (1) is 21 bits, determined as follows:

- 8-bit (signed) value × 8-bit (signed) value = 15 bits
- + 40 multiplied values = 6 bits
- 21 bits

It is well known that high speed digital correlation is a signal processing function that is ideally suited for RNS design techniques [4]. This is due to the fact that RNS arithmetic is extremely efficient in executing high speed addition and multiplication. Furthermore, the modular structure of the RNS leads to modularity in the hardware, thereby facilitating design, construction and testing. This modularity becomes even more important in future VLSI implementations of the correlator.

To prevent overflow during calculation, four 6-bit moduli were selected; 64, 63, 61, and 59. (Note that 64 is allowed since the largest residue from a mod 64 number is 63) This gives an RNS dynamic range of 24 bits which easily handles the largest possible result from (1). The 6-bit moduli were selected because the largest high speed ROMs that are commonly available are 8192 x 8, for a 13-bit address space. This would allow two 6-bit residues to be multiplied or added using a high speed ROM lookup table instead of a more time consuming and complicated hardware multiplier. Use of smaller moduli would not improve the speed but would increase the hardware required; thus, they were not selected.

3. Correlator Hardware
The RNS correlator prototype is composed of several functional units: four RNS correlator channels, a residue
reconstruction unit, echo memory and an Intel 80286 microprocessor. In addition, a Compaq-386 personal computer is used to graphically display the blood flow profile and to program and control the correlator. An ultrasonic scanner is used to identify the desired blood vessel and to generate the echo signal for the digitizer. (See Figure 1)

3.1. RNS Correlator Channel

The residue correlator channel consists of a pipelined architecture which performs an add and a multiply simultaneously for the 40 samples. The samples are encoded into residue form as they enter the pipeline. The arithmetic operations in the correlator channel are performed using a ROM lookup table. Since the product or sum can be at most 6 bits in length, a ROM of size \(2^{21} \times 6\) \((4096 \times 6)\) is all that is required. Each operation can then be performed in the time required to look up the result, which in this case is about 40ns. The system includes 4 correlator channels each of which is architecturally identical and differs only in the contents of the residue encoding and arithmetic ROMs. (See Figure 2)

3.2. Residue Reconstruction Unit

The results from the four residue correlator channels must be reconstructed into a binary value before it can be evaluated. This unit gathers the resultant residues from the four correlator channels and applies the Chinese Remainder Theorem to obtain the binary result. The normal form of the Chinese Remainder Theorem for the chosen set of parameters is:

\[
f(x_{a0}, x_{b0}, x_{c0}, x_{d0}) = \left[ (x_{a0} - x_{d0})_{n_0} + x_{b0} + x_{c0} \right]_{m_0} \mod M \tag{2}
\]

where \(M = (m_0) (m_1) (m_2) (m_3)\), \(n_0 = M/m_0\), and \(x_{a0}^{-1}\) is the multiplicative inverse of \(n_0\) modulo \(m_0\). Although 21 bits are required to handle the full dynamic range of the binary output, the full 21 bits of accuracy are not needed for subsequent processing. Therefore, a scaled output, denoted \(f(x_{a0}, x_{b0}, x_{c0}, x_{d0})\), is produced by applying the scaled Chinese Remainder Theorem as follows:

\[
f(x_{a0}, x_{b0}, x_{c0}, x_{d0}) = \left[ (x_{a0} - x_{d0})_{n_0} + x_{b0} + x_{c0} \right]_{n_0} \mod n_0 \tag{3}
\]

In (3), \(n_0\) denotes the scaled dynamic range, which in this design is 18 bits. The parameters \(n_{03} = n_{02}/m_0\), \(n_{02} = n_{01}/m_0\), \(n_{01} = n_{00}/m_0\) and \(n_{00} = n_{00}/m_0\) are all integers. The one exception, \(n_{03} = n_{00}/m_0\) is made into an integer by rounding \(n_{03}/m_0\) to the nearest integer. After the result is translated into 2's-complement form, only the most significant 16 bits are retained for further processing. This 16-bit result provides adequate precision for further processing and is consistent with a 16-bit integer format used in the Intel 80286 processor. The scaled Chinese Remainder Theorem is implemented by precalculating two subtables (shown in parenthesis in the above equation) and storing them in ROM. The two subtables are then added together and checked for overflow. If an overflow occurs, the result is taken modulo \(n_{03}\). In order to save time, both the result and the result modulo \(n_{03}\) are calculated and the correct one selected based upon the carry out of the adder [5]. (See Figure 3)

3.3. Echo Memory

The echo memory consists of a 256K x 8 dual-port memory with 25ns access time in which two 8-bit samples can be read out simultaneously. This feature is necessary so that the correlator can be performing an operation on every clock cycle. In addition, when writing into the memory, the write port accepts four 8-bit samples per write cycle. Since the samples are written by a 50MHz A/D converter and the memory cannot sustain that write frequency, the write port of the memory was made 32 bits wide so that samples could be multiplexed to make the write frequency more manageable.

3.4. Intel 80286 Microprocessor

The microprocessor is used to control the correlator and run an averaging algorithm on the various correlations performed by the residue correlator channels. The processor initializes the system, calculates and sets the addresses at which to correlate the echo samples and generates flow results which are transmitted to the personal computer for graphical display. A microprocessor is included so that the system can be more configurable and flexible as the blood flow measurement technique is being verified.

4. Results

In the earliest blood flow phantom experiments, the correlations were performed using a small Z80 based machine which performed arithmetic operations at 50ns per operation. Due to the high overhead associated with the equipment supporting this correlator, a single 1-D scan required 15 minutes to compute. With the initiation of the first animal experiments, the system was changed to run completely in software on an Intel 80386 based machine with a Weitek floating point accelerator. This system required approximately 15 seconds to calculate a single 1-D scan. While this represented a vast improvement over the previous system, it was still too slow to gather significant usable data since it was difficult to keep the transducer aligned for that amount of time. The RNS correlator prototype being used for the second round of animal experiments is able to perform a 1-D scan in about 2 seconds. This improvement will allow the sonographer to get far more immediate feedback regarding the proper alignment and placement of the transducer. With the RNS correlator, the blood flow technique can be experimentally verified with animal studies.

5. Future Research

Once the correlator prototype has been verified through blood flow phantom and animal studies, further improvements in performance will be necessary prior to the initiation of clinical verification. To achieve this increase, it will be necessary to integrate the correlator architecture into a single integrated circuit. This circuit will include all the residue channels and the residue reconstruction unit as highlighted in Figure 4. However, if the design is reduced to a VLSI circuit, it will no longer be possible to utilize high speed ROM table lookups for arithmetic operations. In order to maintain high throughput while avoiding the addition of a hardware multiplier, the design will be altered to use a logarithmic approach for performing multiplications. In the modified design, a new set of moduli will be selected consisting of smaller prime numbers, of which more of will be used. This will allow the multiplication operations to be implemented by addition of finite field logarithms and log-antilog tables.
which require considerably smaller ROMs than the complete stored-table lookup operations used in the prototype. Finite field logarithms can be used so long as the moduli are prime integers. Figure 4 shows the new components that can be used to replace the large (8192 x 8)-bit commercial ROMs used for the multiply and add operations in the prototype. The structure shown in Figure 4b is suitable for both the adder and the multiplier. In the case of the multiplier, the lookup tables used encode the 8-bit samples into residue form will be modified to produce the logarithm of the residue directly. Note that this will require only a change in the stored table contents and no additional hardware. An adder then forms the sum of the logarithms and a ROM correction table does both a modular correction and an inverse logarithmic mapping to produce the correct residue product. For the adder, the hardware structure remains the same and the ROM will be programmed only for the modular correction. Two interesting and useful features result from the modified design. First, the large ROM of the original design is replaced with an adder, a latch register, and a much smaller ROM. Second, the latch between the adder and the ROM will allow for a higher degree of pipelining. It is anticipated that the new design will be much faster than the commercial components used in the prototype and that the VLSI chip set that results from this new design will greatly reduce power consumption and increase the reliability of the complete instrument.

Acknowledgements - This work is supported by the National Institutes of Health under grant HL 33704.

REFERENCES


6. Summary

A RNS architecture was selected to provide a high speed real-time processing capability for the hardware correlator used in an ultrasound time domain blood flow measurement system. The RNS correlator has been designed and constructed and is currently being used for detailed verification of the time domain flow measurement technique. It is expected that future work in integrating the correlator into VLSI components will lead to further improvements in performance and allow the initiation of full clinical verification of the blood flow measurement system.

![Figure 1. A block diagram of the correlator system. (Highlighted area intended for VLSI implementation)](image-url)
Figure 2. A block diagram of a RNS correlator channel.

Figure 3. A block diagram of the residue to binary converter.

A) ROMs used in wire-wrapped prototype.

B) New design for VLSI implementation.

Figure 4. Modified designs for RNS Adders/Multipliers suitable for custom chip design and fabrication.