

ULTRASONIC PHASED-ARRAY DRIVER SYSTEM

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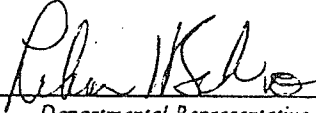
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CHAPTER 1

INTRODUCTION

Cancer is one of the most prominent causes of illness related death in the world today. With already 3000 known carcinogens, it is a problem that requires due attention. However, most attempts for finding a cure have met with very limited success. One of the main reasons stems from the difficulty in targeting a therapy at a cancerous tumor without affecting the vital cells situated nearby.

Hyperthermia may be able to sustain preferential killing of the cancerous tissue by exploiting a tumor's sensitivity to heat caused by its environmental conditions. For example, blood flow is often the sole means of heat removal from the tumor area. However, blood flow rates in tumors tend to be 0.4 times less than that in normal tissue [1]. Furthermore, some tumors lack the normal homeostatic response that causes an increase in blood flow with an increase in temperature; this aids heat conduction away from the area [2]. Other conditions which can sensitize the tumor to heat are nutrient depletion and an acidic environment.

One of the main problems associated with current hyperthermia treatments has been the inability to deliver the necessary heat to tumors without any unacceptable heating of the normal tissue. According to Samulski, the main reason that hyperthermia has failed to live up to its promise shown in previous biological experiments is "the technical difficulty of elevating tumors to appropriate temperatures and determining the

temperature distributions obtained. . . there is an insufficient effort in developing appropriate equipment [3]."

One device that holds great promise in this area of controlled heating in several superficial and deep lesions is the ultrasound phased-array. Taking advantage of the short wavelengths that can be used with ultrasound, phased-arrays allow focusing characteristics that are unparalleled in other current, noninvasive modalities. There are several other advantages offered by phased-arrays. First, microprocessor controlled phased-arrays have excellent control of their focus and can allow excellent localized heating patterns by steering their beam around a tumor's periphery. This microprocessor control is especially beneficial if the acoustic window or the tumor has a complex or asymmetric shape and requires easy modification of the scanning pattern. In cases where the tumor is confined to scattered areas or deep-seated volumes, there is often no other practical alternative to ultrasound phased-arrays for hyperthermia treatment. Often it is these deep-seated tumors which are the most life threatening [4]. This can be compounded with complications in the surgical removal of the tumor due to its inaccessibility. It is in cases such as this where noninvasive hyperthermia is the most advantageous.

Recent technological advances have renewed interest in localized hyperthermia. Noninvasive imaging, such as positron emission tomography may be used to investigate the blood flow in various areas. This gives an improved thermal mapping of the tumor vicinity and will allow hyperthermia to be used to its full capability. Utilizing phased-arrays, treatments can be administered

with less occurrence of undesirable cold spots which are often attributed to treatment failure.

There are several potential problems with phased-arrays. The large number of elements in phased-arrays require a significant number of amplifiers. These amplifiers require a complicated controller that should allow the scanning patterns to be readily changed to suit the treatment conditions. Also, electrical coupling between the driving signals of the elements will become prominent at high frequencies largely due to the capacitive reactance of the transducers [5]. The primary objective of this thesis research is directed toward the solution of these problems in the process of designing and implementing an ultrasound phased-array driver system.

CHAPTER 2 SYSTEM OVERVIEW

2.1 Design Objective

The main objective of the Ultrasonic Phased Array Driver System (UPADS) is to generate the desired excitation signals for all of the elements in a phased array. As a laboratory prototype, the system should be extremely versatile so that it may be used with several different applicators. Finally, although the large number of elements demands a significant amount of hardware, much of it is redundant so that the system should be designed with easily reproducible components.

2.2 Design Specifications

There are certain specifications that become evident from the design objective. First, consider the requirements for driving different applicators:

1. Since each applicator may have a unique resonance frequency, the driving system must allow various operating frequencies.
2. Since the applicators may have different efficiencies, the system should have an adjustable power output.
3. Since each array may have a different number of elements, the number of active drivers should be controllable.

4. Because each element will require a specific matching network depending on the array, the system should allow interchangeability of these circuits.

Second, in order to facilitate analysis of different phasing techniques,

1. The system should simultaneously output all of the signals to the phased array.
2. The transition time between focal points should be minimized.
3. The system should always be accessible for emergency shutdown.
4. There should be an easy means of loading data into the system since its record size is large.

Finally, in order to facilitate the realization of the system,

1. The system should be subdivided into modules according to their functions to simplify system repair and debugging.
2. All of the modules should share a general form for simple reproduction since there is some redundancy in the system.
3. The system should be expandable so that arrays with more than 64 elements can also be driven.

2.3 System Description

UPADS consists of 5 major components. They are,

1. User Interface
2. System Bus

3. Digital Control Circuits

4. Amplifier Circuits

4. Matching Circuits

The user interface allows the user to enter the desired amplitude and phase of each element's driving signal on a personal computer (PC). This can be done via keyboard entry or flat ASCII file on a floppy disk. Once the PC has processed and converted the data to binary, the data will be outputted by a Direct Memory Access (DMA) card onto the system bus, which delivers the data to the Digital Control Circuits (DCC). The main role of the DCC is selecting the specified data for each element from the system bus, converting it to a square waveform with the desired duty cycle and phase, and inputting the waveform into the amplifier circuits. It is the amplifier circuits' responsibility to increase the voltage to a level suitable for driving the piezoelectric transducer elements. The signals are then sent from the output of each amplifier through a separate component of the system bus to its corresponding matching network, which is utilized to cancel the reactance of the transducer element so that the amplifier can drive a resistive load.

2.4 Practical Considerations

A prototype system with 64 channels was constructed to the specifications mentioned above. Due to space limitations and for reasons that will become clear later, the drivers were divided into modules with only 8 channels. Accordingly, the matching networks were grouped in modules of 8 and connected to the amplifiers by an in-house bus. The module concept is helpful in

repairing the system. Because each module is identical, if an amplifier module is not operating correctly, it can be easily replaced with another one. Also, it facilitates system debugging by allowing it to be done on both the system and module levels. These modules were designed and laid out on printed circuit boards (PCB). This allowed the circuits to be easily reproduced, made the system more reliable, and minimized differences in response between channels.

CHAPTER 3

DIGITAL CONTROL CIRCUITS

3.1 Design Objective

As was noted in the Introduction, the implementation of 64 square waves with specified amplitudes and phases is crucial to the operation of a phased array. This is accomplished by the Digital Control Circuits (DCC) outputting to MOSFET amplifiers (discussed in Chapter 4), which elevate the signals to a level capable of driving the individual elements in the array. Note that although most of the numerical conversion takes place in the personal computer (PC), the actual waveforms are generated by the DCC.

3.2 Design Specifications

The DCC has several design specifications which are necessary to satisfy the design objective

1. In order to preserve the phase information, the DCC should have a parallel output to all of the elements for a specific focal pattern. A sequential output of the waveforms will have an inherent phase error due to the relative time delay.
2. The DCC must be accessible by the DMA to either output another focus or shut down the system.
3. If the scanning method is used to acquire the desired heating pattern, and the dwell time for each focal point is used to compensate for intensity loss, the time averaged intensity of the scanned field can be given by Equation (3.1):

$$I_{av}(x, y, z) = \frac{1}{T_s} \sum_{l=1}^{N_f} I_l(x, y, z) \Delta T_l \quad (3.1)$$

where T_s is the scan period, N_f is the number of focal points, $I_l(x, y, z)$ is the field intensity profile of the l th focal point and ΔT_l is the dwell time at that point [6]. In order to maintain the maximum possible dwell time at each focal point, the DCC should continue to generate waveforms up to the output of the next focal point.

These features will be discussed throughout this chapter.

3.3 Circuit Description

3.3.1 Variable amplitude phase shifting network

The central component of the DCC is the Variable Amplitude Phase Shifting Network (VAPSN). The remaining circuitry is to control the VAPSN and to synchronize the DMA. The VAPSN consists of 64 clusters of two 74LS193 synchronous up/down four bit counters and a 7402 dual input NOR gate allowing each cluster to independently synthesize a waveform. See Figure 3.1. (All figures appear after Chapter 8.) Only the most significant bit (MSB) output, QD, of each counter is used. When the system clock is connected to the count-up input of the counter, the MSB output will be high for eight clock cycles and low for eight clock cycles. This constitutes a 50% duty cycle square wave with a period equal to sixteen clock periods. Thus, the operating frequency of the system can be given by $f_{system} = f_{clock}/16$.

The transistor-to-transistor logic synchronization (TTL SYNCH) output of a Hewlett-Packard (HP) 3325A waveform

synthesizer/function generator is used as the system clock. Thus, the system is extremely versatile in that it can drive phased arrays with different resonant frequencies. The outputs of both counters are sent to the dual input NOR gate that outputs a high only when both inputs are low. Thus, by controlling the duration of time when both counters are low, the system may implement square waves with desired duty cycles. Figure 3.2 shows how a square wave with an 18.75% duty cycle might be generated.

This control is implemented by programming each counter's preset inputs, which are used to set the initial state of the counter. Loading the presets causes a counter in the count-up mode to count from this initial state up to fifteen and then repeat the cycle of counting from zero to fifteen until the next load. Figure 3.3 shows the shifted outputs of a counter using different presets. Let the assigned reference signal be the output of the counter with a preset of 8 (1000 in binary). If the preset, P , of another counter is set between 0 and 8, the result is a 50% duty cycle square wave that lags the reference signal by $(8 - P) \times 22.5^\circ$. If the preset is between 9 and 15, the output will be the same square wave but leading the reference signal by $(P - 8) \times 22.5^\circ$. If the + and - notation is used to represent leading and lagging, respectively, then the phase is given by $(P - 8) \times 22.5^\circ$. Figure 3.4 displays how this phase shifting technique can be used to construct two waveforms that are 180° out of phase.

As was mentioned previously, the outputs of both counters in the cluster are sent to a NOR gate. The second counter is used to control the duty cycle. In order to control the duration that both

outputs are low, the second counter's preset must be set relative to the first counter's preset. Therefore, the first counter in the cluster is used to set the relative phase with respect to a reference signal while the second counter in the cluster is used to set the duty cycle. Both the phase and amplitude information are actually a function of the two presets. This is illustrated by Figure 3.5, which shows the presets needed to implement a waveform with a duty cycle of 25% and a phase shift of 135° with respect to a reference signal generated by a counter which was preset to 0. In addition, the maximum duty cycle of 50% is obtained by taking the NOR of two identical waveforms. A duty cycle of 43.75% can be achieved by taking the NOR of waveforms outputted by counters with presets that differ by one. Furthermore, an element can be inactivated by setting the presets so that they differ by eight. As a result, only one of the two counters will be low at any time, causing the NOR gate to always output a low signal.

It is readily apparent that only eight duty cycles can be achieved by this system. Thus, although 8 bits are necessary to specify a certain phase shift and duty cycle, there is, in actuality, only 3 bits of resolution for the duty cycle and 4 bits of resolution for the phase, as was shown by the 16 waveforms in Figure 3.3. Also, it should be noted that one waveform is necessary as a reference.

3.3.2 Variable amplitude phase shifting network control circuits

The Variable Amplitude Phase Shifting Network Control Circuits (VAPSNCC) is responsible for gating the data from the DMA into the presets of the counters. (See Figure 3.6.) The data for each focal pattern consist of 64 eight bit words (four bits per counter). In addition, addressing bits are necessary for data selection from the bus. Because working with this data record was too cumbersome, the data was broken into smaller packets, one per cluster. Each packet contains one eight bit datum and a corresponding eight bit address word for addressing the selected cluster. These packets are outputted sequentially by the DMA onto the STD bus. Thus, in order to generate all of the signals required for a single focal pattern, the data for each cluster must be loaded one at a time, beginning with cluster 0 and ending at cluster 63.

The stipulation that the DCC should simultaneously output all 64 waveforms necessitated the use of clocked storage for each cluster. Holding registers, implemented by 74LS374 Octal D-type Flip-Flops which require no complicated handshaking for loading, serve this function well. The data is downloaded from the DMA onto the bus. After a delay which allows the data to stabilize, the address word is inputted to the control circuits, which subsequently clock the corresponding register, causing it to take the state of its inputs. This process is then repeated until all of the remaining registers have been loaded. Note that the data at the D-type Flip-Flop outputs will remain latched at their present state until a register is clocked again. Because each of the registers' inputs are

placed on a common bus for all 64 clusters, the control circuits need to clock only the selected cluster register when its respective data is on the bus, so that the other 63 registers are in no danger of loading in the incorrect data.

The address word is comprised of four bits used for addressing a specific board in the system and the three bits used for selecting a particular cluster on a board. Thus, the system's configuration has a maximum of sixteen boards with eight clusters residing on each board. The board address is set via a four bit hexadecimal hybrid rotary dip switch and implemented by an on-board four bit magnitude comparator. The comparator, a 74LS85, compares the address set by the switch with the four bits in the address word allocated for board selection. In the event of a match, the comparator sends a logic level high signal to the A=B output, which is tied to the active high enable of a three to eight decoder (74LS138) of the selector board. Once enabled, the decoder outputs a logic level low signal to one of the eight clusters, which is selected using the three bits allocated for cluster selection. Each decoder output is tied to its respective register's clock. Thus, when a specific cluster's data comes on line, a comparator selects the correct board and enables a decoder which clocks the corresponding cluster's register, loading it with the specified data. The DMA then outputs the next cluster's data and the process repeats until the remaining registers have been loaded.

Since the outputs of each register are tied directly to the presets of the two counters in its respective cluster, to update the presets with the data stored in the register, the DMA needs only to

output a common logic level low load command in the address word (1 load bit) to all of the counters. (In order to avoid confusing this load with the load outputted by the addressing network to the registers, the former will be referred to as the startup command.) The startup command overrides the system clock and forces the counters' presets to take the state stored in the register. This is called a jam load. When the load signal goes high, the counter will count with every positive edge of the system clock. However, this load is asynchronous to the clock and thus can occur anywhere along the clock cycle. It is, therefore, possible that the load goes high at approximately the same instant as the count-up clock goes high. On this occasion, the required setup time for the enable input (removal of the load signal) will not be satisfied. The setup time is defined as the amount of time that an input is required to be stable before another event can occur. In this case, the removal of the load occurs too close to when the count-up signal is applied. According to its data sheets, the 74LS193 will operate in the guaranteed mode at clock speeds around 25 MHz. The minimum load inactive-state setup time, t_{SU} , for the 74LS193 is approximately 15 ns. If the system clock is running at 12 MHz, this setup time corresponds to approximately one-fifth of a clock period. Thus, it is readily apparent that the load inactive-state setup time will not be met if the count-up goes high within 15 ns after the load has been removed. This event could create a metastable state; for the same clock input there are two possible counter outputs. The counter could either count up with the positive edge of the clock, or count up with the next positive edge.

Since the counters are not operating in the guaranteed mode, the output of two counters receiving the same input could be different. Thus, a counter that was preset for a one count difference with respect to another counter could have, in actuality, a zero or two count difference. In this application, this translates into either

1. A square wave with a duty cycle that is 6.25% shorter or longer in duration than the intended duty cycle.
2. A cluster output that is shifted 22.5° with respect to its intended phase.

Since the phase information is extremely important to the operation of phased arrays, this phase error could seriously degrade a synthesized focal pattern that is both asymmetric and complex [7]. There are two possible remedies to this problem

1. If the count-up input of the counter was gated, it could be held high during the load sequence. After the load becomes inactive, the count-up input will go low on the next negative edge of the clock. This would give the load-inactive state one-half of a clock period for setup time. This setup time should suffice if the system clock is 12 MHz or less.
2. The second solution uses almost the same scenario as the first one except that it gates the load signal. If the load signal is synchronized with the negative edge of the clock, it would give the load one-half of a clock period before the count-up signal (clock) goes high. Once again, this should give ample amount of time for the setup of the load-inactive state. The second solution gives the same result

as the first solution but is somewhat easier to realize. Thus, this solution is implemented in the Load Synchronization Circuit, LSC (enclosed in the dashed lines in Figure 3.7.)

Because the load for the 74LS193 counters is an active low signal, the load-inactive state occurs on the positive edge of this signal. The positive edge of the load must be synchronized to the negative edge of the system clock which feeds the count-up of the counter. This can easily be done using D-type flip-flops, and there are several advantages to using them. First, unlike RS flip-flops, the D-type flip-flops have direct inputs such as a reset and a clear which do not require a clock pulse. Second, the D-type flip-flops are edge-triggered unlike most standard JK flip-flops which are level-triggered. Level-clocked devices require complicated timing sequences to ensure that the input states do not change when the clock is gating data. Thus, JK flip-flops require additional combinational logic to strobe the data in correctly.

Hence, a D-type flip-flop such as the 74LS74 would be ideal for triggering a signal to a certain edge of the clock pulse. The only drawback is that the 74LS74 is a positive edge triggered device. This is overcome easily by inverting the clock pulse and feeding it into the clock of the 74LS74. Thus, although the 74LS74 is still triggering on the positive edge, it is in actuality triggering on the negative edge of the system clock. With the active low load signal fed into the input, D, of the D-type flip-flop, the output, Q, will go low on the negative edge of the system clock. It should be noted that the D input remains asynchronous to the clock. Thus, it is still

a possibility that the DMA load signal could go high at the same instant that the inverted clock goes high. In this case Q could either take the same state as the input on this positive edge or do so on the next clock pulse. Therefore, the output could be delayed by one clock pulse. However, this still will not cause a problem since the output of the flip-flop is common to all of the counters in the system and is synchronized to a negative edge of the clock. Therefore, all of the counters in the system will see the same signal and have adequate setup time. The only effect that this metastable state will have is a maximum delay of one clock period in the loading of the next subsequent focal pattern into the presets of the counters. With a clock frequency of 12 MHz, this delay is approximately 83 ns. For all practical purposes, this is almost negligible compared to the actual dwell time of the focal pattern.

The output of the D flip-flop is sent to all of the boards along the synchronized load bus using line drivers (74LS244) whose output is tied to the clear input of a 74LS74 on each board. When the on-board 74LS74 receives the low load signal at the clear input, it will output a logic level high signal from \bar{Q} . This output is then fed into four inverters that in turn drives the load inputs of the sixteen counters. The inverters are necessary to give the required logic level low signal and also to avoid exceeding the fanout limit of the D-type flip-flop.

The DMA may need to access the DCC to serve one of two functions. If the scanning method is being used for local heating, the DMA will need to access the DCC each time it outputs a focus. Since the DCC acts as a peripheral that is always in the listen mode,

to access the DCC, the DMA needs only to output the data onto the bus. With no other talkers on the bus other than the DMA, handshaking is unnecessary. As the only device that is in the listen mode on the bus, the DCC receives everything that is downloaded onto the bus. The VAPSNCC waits for the address and upon its arrival clocks whatever is present on the data bus. The 16-bit output of the DMA is set up so that the 8-bit data word goes out first and stabilizes before the 8-bit address word is sent out. The second function stipulated in the circuit specification of immediate shutdown can also be realized by sending a preprogrammed output of the 0% duty cycles. Note that this and any other output can be sent without causing the system to glitch because the LSC synchronizes all outputs and allots the proper set up time.

The requirement that the output of the DCC be continuous is satisfied because the counter only utilizes the presets for the first cycle of counting to set the initial phase shift of each cluster's output. Since the counter receives the new state of the presets only when the startup signal is present, the registers can be changed to load the next focal pattern without affecting the counter upon removal of the signal. The only time the counters stop is during the startup command. Since the duration of this command is relatively small with respect to the average time constants attributed to tissue, the output can be considered continuous.

3.4 System Hardware

3.4.1 Variable amplitude phase shifting network

The hardware used to construct the VAPSN is listed below:

1. 16 - 74LS193 4-Bit, synchronous binary up/down counters.
2. 8 - 74LS02 Dual input NOR gates.

The 74LS193 offers a synchronous mode of operation with 4-bit parallel load presets. There are several inherent advantages to using synchronous counters as opposed to asynchronous (ripple) counters. In a synchronous counter, all stages are clocked simultaneously by the steering logic which causes the stage outputs to change coincidentally with each other. Asynchronous counters are somewhat slower because each stage (flip-flop) of the counter must be clocked by the output of the stage preceding it, which results in an accumulated propagation delay. Also, output current spikes are commonly associated with ripple counters.

3.4.2 Variable amplitude phase shifting network control circuits

In order to implement the VAPSNCC, the following hardware was used:

1. 2 - 74LS244 Octal tristate noninverting drivers.
2. 1 - 74LS138 3 to 8 line decoder.
3. 1 - 74LS85 4-Bit magnitude comparator.
4. 8 - 74LS374 Octal D-type flip-flops.
5. 5 - 74LS04 Inverters.
6. 1 - Hexidecimal Hybrid Rotary Dip Switch.

The following is a list of the TTL IC's used to implement the LSC.

1. 2 - 74LS74 Dual D-type flip flop with preset and clear.
2. 6 - 74LS04 Inverters.

Low power Schottky (LS) TTL was used for all IC's in the DCC. It offers speed comparable to the standard 74 series TTL with considerably less power consumption. There is a tradeoff however: 74LS is more sensitive to ground level noise spikes than the standard 74 series.

3.5 Practical Considerations and Future Recommendations

When implementing a logic design and interfacing TTL IC's, the main design considerations are the prevention and elimination of noise. There are several reasons for this. First of all, the fairly low output signal level and noise margin make the TTL IC's extremely sensitive to noise introduced from external sources, power supplies, and switching noise. Secondly, TTL IC's are inherently noisy. Finally, since an interface often shares a common ground with the digital circuits, noise from the interface may pose a problem to the operation of the TTL IC's.

Since output can typically be 2.4 V for a logic high and 0.4 V for logic low (nominally 3.5 V and 0 V, respectively) with threshold input voltages of 2.0 V (V_{IL} maximum) and 0.8 V (V_{IH} minimum). Therefore, the noise margin for either logic level signal is possibly 0.4 V, although gates normally have a noise margin on the order of 1 V [8]. Any input between V_{IL} maximum and V_{IH} minimum will produce an unpredictable output. Thus, it is possible that noise

introduced to one logic level signal could make it to appear as the other logic level signal. Since the noise related problems are often intermittent, finding solutions to them may be time consuming and difficult. One possible approach is to discover and eliminate the sources of noise.

The two major sources of noise in the UPADS are the TTL circuits and the CMOS amplifier circuits. The noise source of the TTL circuits can be found in their output stages. Transistor-to-transistor logic employs a totem pole output stage, characterized by a pair of output transistors tied between the power supply rail and ground. Its operation is similar to a push-pull circuit. When the upper NPN transistor is biased, the output swings to the V_{CC} and pushes (sources) current; when the lower NPN transistor is biased, the output swings to ground and pulls (sinks) current. While this output stage possesses distinct advantages over pull-up type output stages, it has a major disadvantage. As the output goes through a state transition, both transistors will be active for a short amount of time. This presents a low impedance pathway between V_{CC} and ground which allows a large current to flow into the ground from the power supply rail. The end result is a current pulse as large as 50 to 100 mA traveling along the ground line [9]. This current pulse when introduced to lead inductances and path inductance on the PCB, could cause significant voltage spikes on the supply rails. Assuming a lead inductance of $0.1 \mu\text{H}$ (which is a fairly good representation of a 6" PCB trace) and a current spike of 20 mA with a duration of 5 ns, (for illustrative purposes, the typical values for a TTL gate are used to compute the amplitude of a possible noise

pulse.) the voltage given by $V = L(di/dt)$ is 0.4 V. This completely eliminates the working noise margin of TTL. Since these current spikes will only supplement each other, it is possible that with only a few gates switching (especially if their switching is synchronous), a TTL circuit could be rendered useless by its own noise. Unfortunately, since these output stages are intrinsic to the TTL gate, there is very little that could be done to eliminate this noise source. The only other viable alternative is to reduce the ground inductance as much as possible. This was done by using a combination of ground buses and ground planes wherever possible.

The second and probably the most prevalent source of noise is the MOSFET amplifiers. Their output stages suffer the same fate as the totem pole output stage of the TTL IC's since there is a period of simultaneous conduction in both gates during a transition. This rush current is extremely large since the MOSFETs have an extremely low on resistance ($r_{DS} = 0.5 \Omega$). This, combined with the high operating voltage of 100 V, results in massive current spikes on the ground rail. In order to eliminate the spikes caused by the amplifier, simultaneous conduction of both gates must be prevented. However, since the gates are controlled by the same input signal, it is clear that this is not a trivial task. The circuitry required to drive the high input capacitance of the power FET will also contribute to this noise since it must source and sink large currents. These considerations will be discussed further in Chapter 4.

Since it was not possible to completely eliminate the noise at the source, the mechanism of how such spikes cause an incorrect signal was analyzed so that a means of prevention could be

developed. It has been already concluded that there will be large current spikes traveling along the grounds due to the switching of both the TTL gates and the amplifiers. A possible situation of how these spikes can affect the outputs is now proposed. Suppose there are 2 gates, A and B, where gate B is adjacent to a noise source. Let gate A drive gate B with an active low signal. If a current spike occurs at the noise source, it will propagate along the ground past B and towards A. Since there is a parasitic inductance in the ground line, this current spike causes a voltage spike which increases as it travels along the ground. Recall that when the output of a gate is low, the output of the NPN transistor and thus the TTL gate is saturated and is connected to ground. Thus, if a voltage spike is present on the ground of gate A, then it will appear on its logic level low output. Since gate B is a closer reference to ground, the spike on the low output of A could actually appear to B as a logic high level pulse, thus causing B to output an incorrect signal. In the UPADS this could cause an improper duty cycle or phase shift.

Several steps were taken in the attempt to minimize such current spikes. As a mandatory first step, one decoupling capacitor for every two IC's was placed as close as possible to the individual IC's on the supply rails. This form of decoupling uses capacitances as a frequency dependent impedance (where $Z = -j/(\omega C)$). Since the frequency of the spikes is roughly known, the capacitor was chosen so that its impedance at this frequency is minimal. Placing these capacitors across the +5 V and ground should effectively remove any high frequency spikes. Also by liberally using these bypass capacitors on the power supply rails the effective path a spike can

travel is reduced. This lowers the inductance which in turn results in smaller voltage spikes. Furthermore, ceramic capacitors which have characteristically low inductances were used for this form of decoupling. This solution alone was sufficient to suppress the voltage spikes caused by the switching of the TTL gates. Thus, it allowed the proper operation of the DCC at low output levels of the amplifier. However, as the output of the amplifiers was increased, incorrect outputs, or glitches, began to reappear. This indicated that the spikes caused by the amplifiers when operated at high output voltages constitute the major source of noise.

There are two possible solutions to the problems due to the current spikes generated by the amplifier. The first solution involves minimizing the current spikes themselves. This was accomplished by using current limiting resistors and decoupling capacitors. Since the current spikes are due to a large rush current that flows from the high voltage rail to ground during simultaneous conduction of both MOSFETs, this current was reduced using current limiting resistors at the sources of both MOSFETs. Using $11\ \Omega$ resistor reduced the magnitude of the current spikes from 1 A to 0.434 A at an operating voltage of 10 V. Since this is still a sizeable current, two forms of decoupling were used. The first form of decoupling is identical to the one proposed above.

Since the frequency of the spikes is a known parameter ($f_{\text{spike}} = 2 \times f_{\text{system}}$), the decoupling capacitor was chosen such that the impedance is minimized at that frequency. The second form of decoupling utilizes capacitors as an energy storage device. The energy stored in a capacitor is given by Equation (3.2):

$$U = .5 (CV^2) \quad (3.2)$$

where U is the energy stored in joules, C is the capacitance in farads, and V is the voltage in volts. Since a capacitor will resist any change in voltage, it is an effective means of voltage spike suppression. For example, if a $10 \mu\text{F}$ is presented with a current spike on the order of 100 mA over a duration of 20 ns , the effective voltage change as given by Equation (3.3):

$$\Delta V = (\Delta I \times \Delta t)/C \quad (3.3)$$

is only 0.2 V . Since this type of decoupling requires large capacitances, (evident in Equations (3.2) and (3.3)) tantalum capacitors, which have relatively large capacitances in small packages, were used for this application. The tantalum capacitors, when placed abundantly along the power buses, will act as local voltage sources, thus regulating these power supply rails.

The second solution involves minimizing the effect of these current spikes on the DCC. In order to do this, an attempt was made to prevent the spikes on the amplifier ground from reaching the DCC ground by isolating the two grounds. Unfortunately, when interfacing analog and digital circuits, a common ground is necessary as a reference in order to establish a switching threshold that is compatible with both circuits. Thus, if the digital circuits are used to switch the analog circuits, the reference is required such that the voltage outputted by the digital circuits will definitely switch the analog circuits. This may not be the case if the ground is removed and the circuits are floating with respect to each other.

The easiest and most effective means of isolating the ground is by using optoisolators. Basically, optoisolators provide an optical transmission link rather than an electrical link, thus eliminating the need for a common ground. Simple optoisolators employ light-emitting diodes as a front end and use photo-Darlington transistors to convert the optical signal to an electrical one. Because this completely eliminates any common mode noise such as ground spikes, it should definitely be used in future designs. Also, it may simplify layout and increase isolation if the amplifiers are located on a different board than the control circuits. The control circuits signal could be sent out along the bus and buffered by optoisolators placed at the input of the board.

Since incorporating optoisolators would require physically altering the PCB, the ground mecca technique was used instead. This technique utilizes individual grounds for different applications and connects them at a common point. In the UPADS, there are dedicated grounds for the digital circuits, amplifier circuits, and the chassis connected only at the main power supply. Thus, any spikes caused by the amplifiers must first travel to the power supply and then back along the digital ground in order to cause a glitch. The combination of the power supply's voltage regulators and the ground mecca's tie with earth ground is normally sufficient to dampen out any voltage spikes. This resulted in better noise immunity for the digital control circuits operating with output voltages in the vicinity of 50 V. However, even with the above modifications, there remained some occasional glitches.

The final step is to apply the understanding gained from the second step to the actual circuit. This mechanism indicates that active low inputs are most prone to noise spikes. By using a state detector at the inputs to the counter, it was determined that the glitches were due to improper presets. The inputs and outputs of the octal D-type register which buffers this data were then examined. This test showed that although the inputs received seemed to be correct, the data stored in the register was not: this implies that the data is corrupted as it enters the register. Since the noise mechanism indicates that active low inputs are susceptible to noise, the active low clock input of the 74LS374 was examined. This input is controlled by the 3 to 8 decoder which outputs an active low signal. Spikes on this signal could be interpreted as the rising edge of the load. If the spike occurs close to the falling edge, this may reduce the duration of the clock signal to an amount smaller than the valid hold time. On the other hand, if the output of the decoder is high, a negative going spike on the output from the +5 V could be interpreted as a low pulse causing the register to clock in the data intended for another amplifier. A plausible solution to this problem involves the introduction of a lowpass RC network at all of the Schmitt trigger clock inputs of the 74LS374. Since the actual signal frequency is fairly low, the 3 dB cutoff frequency was set for approximately 10 kHz. This Schmitt trigger filter effectively removes both positive and negative going spikes so that the occurrence of glitches are reduced. As a result, stable operation of the system may be achieved driving a resistive dummy load of 75 Ω . These modifications should be sufficient for the proper operation of

the system when driving the phased array applicators through matching networks. As an added insurance, the presets can be constantly refreshed using the DMA. Thus, any glitches that may occur could be corrected by the DMA during the next refresh cycle.

CHAPTER 4

AMPLIFIER CIRCUITS

4.1 Design Objective

The amplifier circuits are necessary to convert the TTL low level control signals to a level capable of driving the piezoelectric transducer elements in the array. According to the piezoelectric effect, the element's surface displacement is proportional to the voltage placed across it. Thus, in order to drive these transducers, the amplifiers should operate as a logic level controlled voltage source. Since the transducer material, lead zirconate titanate, presents a complex impedance, the amplifiers should be able to drive reactive loads. Although these elements will be matched in the final implementation, it would be useful to drive them without any matching circuits in preliminary experiments so that the actual voltages placed across the elements and the effects of the matching circuits would be known. Finally, since the system will be used to drive various phased arrays, the amplifier's power output should be large enough to drive the least efficient applicator.

4.2 Design Specifications

In order to implement the design objective, the amplifier circuits must have certain characteristics

1. Since the input to the amplifier is a signal from a NOR gate, a gate drive circuit is required to translate the TTL level

signal to a level which is capable of driving the MOSFETs to saturation.

2. Since the large input capacitance of the power MOSFET is driven by a square wave with fast transition times, a drive circuit is required to source and sink large transient currents.
3. Because the amplitude information is represented by the duty cycle of the TTL signal, the output of the gate drive circuit should maintain this duty cycle.
4. The amplifier should act as a voltage source capable of driving the reactive loads in the elements of the phased arrays.
5. The power output of the amplifier must be adjustable in order to account for the various efficiencies of different phased arrays as well as allowing the acoustical power output of a specific array to be controlled.

4.3 Circuit Description

The amplifier used in the UPADS switches between $V^+ = 100\text{ V}$ and $V^- = 0\text{ V}$ as its logic level input changes. This section will compare MOSFET and bipolar transistors and analyze the amplifier used in UPADS.

4.3.1 Comparisons of MOSFETs and bipolar power transistors

In implementing this amplifier, there are two types of power transistors that could be used: the bipolar and the MOSFET. When

compared with power bipolar transistors, power MOSFETs offer some definite advantages. Power MOSFETs have a higher speed capability, fewer problems with thermal runaway and secondary breakdown, and a lower noise figure. However, in certain applications there are several distinct disadvantages in using power MOSFETs. Particularly, there is the problem of simultaneous conduction of both power MOSFETs in a common drain configuration.

Power MOSFETs have superior switching speeds to bipolar power transistors since they are respectively majority and minority carrier devices. Power bipolar transistors have an inherent storage time since they must remove the minority carriers stored in the base. However, since the MOSFET is a voltage controlled device, its transition time is only a function of the charge and the discharge of the gate capacitance. In turn, power MOSFETs with higher switching speeds are more efficient at higher frequencies. This is crucial for MOSFETs operating in the common drain configuration since short switching times will minimize the duration that the rush current is drawn.

The power bipolar transistors are more susceptible to thermal runaway than the MOSFETs. If the base-emitter voltage, V_{BE} , is constant, an increase in temperature causes an increase in collector current, I_C , which further increases the transistor's temperature. This sets up a positive feedback loop which results in thermal runaway that may eventually lead to transistor destruction.

In comparison, power MOSFETs exhibit fewer problems with thermal runaway. The drain current, I_D , of a N-channel MOSFET in saturation is given by Equation (4.1):

$$I_D = k (V_{GS} - V_T)^2 \quad (4.1)$$

where V_{GS} is the gate-to-source voltage, V_T is the threshold voltage, and k is the conductivity parameter given by Equation (4.2):

$$k = 0.5 \mu_n C_{OX} (W/L) \quad (4.2)$$

where μ_n is the electron mobility in the induced N-channel; C_{OX} is the capacitance per unit area of the gate-to-channel capacitor with the oxide layer serving as a dielectric; W and L are respectively the width and length of the channel. According to Equation (4.1), V_T with its negative temperature coefficient will cause the drain current to increase when the temperature is increased. Although the conductivity parameter k also has a negative temperature coefficient, it will cause the drain current to decrease with an increase in temperature. The magnitude of V_T only decreases about 2 mV for each Celsius degree rise in temperature [10], while the temperature coefficient of k is quite large and is given by $k \propto T^{-(3/2)}$. With large drain currents, the overall effect of temperature on the drain current will be dominated by k . Thus k , with its negative temperature coefficient, will counter the increasing drain current, eliminating any possibility of thermal runaway. The on resistance of a MOSFET, $r_{DS(on)}$, with its positive temperature coefficient, limits the current as the temperature increases. This will also contribute to temperature stability. Besides, the switching speed of the MOSFET, which is mostly a function of the gate capacitance, is relatively independent of temperature. The switching speed of the power bipolar transistors, on the other hand, will decrease with the increase in temperature, resulting in higher dynamic losses. Thus, it is evident that the

power MOSFETs have more favorable temperature characteristics than the bipolar transistor.

Secondary breakdown occurs because there is a nonuniform current flow across the base-emitter junction of a transistor that results in a high current density near the periphery of the junction. This increases localized power dissipation which will raise the temperature in the so-called hot spots. Since an increase in temperature causes a larger current, a form of thermal runaway, eventually ending in the destruction of the junction, will occur [11]. Fortunately, this phenomenon does not happen in power MOSFETs operated within the given ratings of the device. In addition, bipolar transistors, depending on the voltage, will require an additional margin for internal power dissipation [12]. However, this is unnecessary if the power MOSFET is operated within its safe operating area (SOA), which is solely determined by its power handling capabilities, peak current ratings, and breakdown voltage. Thus, MOSFETs allow simpler power considerations and less stringent circuit designs.

Finally, the noise figure of MOSFETs is lower than bipolar transistors. The two types of high frequency noise common to transistors are shot noise and thermal noise. Shot noise is a side effect of forward biased junctions; since MOSFETs do not possess any forward biased junctions, this is nonexistent. Thermal noise, due to moving carriers upon the flow of electrons, equally affects both transistors. Thus, the MOSFETs' total noise figure is smaller than that of the bipolar transistors. From the above comparisons, the MOSFETs are better suited for this system.

4.3.2 Analysis of amplifier circuit

Although the components of the amplifier circuit operate in unison to produce the required output signal, for descriptive purposes, they have been classified in terms of the functions they perform: they are the gate drive circuit, the output stage circuit, and the level shifting circuit. See Figure 4.1.

4.3.2.1 Gate drive circuit

Since power MOSFETs are relatively new innovations, there has been no recent developments in circuits designed specifically for MOSFET gate drive applications. However, other interface IC's can be easily adapted to serve this purpose. The integrated circuit used to implement the gate drive circuit is a DS0026 5 MHz two-phase MOS clock driver manufactured by National Semiconductor. The DS0026 possesses the desired characteristics: TTL input compatibility, high current drive, and pulse width controllability. These characteristics will now be discussed.

First, the DS0026 features TTL compatible inputs which can control an output swing of 20 V. When the input is a logic level high, the output will be connected to V^- ; when the input is a logic level low, the output will swing to V^+ . Although the DS0026 acts as an inverter, because the output stage is also an inverter, there will be no overall effect on the duty cycle of the output signal. For this system, the V^+ is connected to a +15 V power supply rail and the V^- is attached to ground. Although the V_{GS} threshold is +2 V and -2 V for the P-channel and the N-channel MOSFETs, respectively, the large

voltage swing ensures that both FETs will be operating in the saturation mode.

The gate driver actually determines the switching speed of the MOSFET since its current will act to charge and discharge the gate capacitance. Thus, the DS0026's high output current drive capability (up to 1.5 A) allows it to drive large capacitive loads found in power MOSFETs even while operating at extremely high speeds. For example, the DS0026 features 20 ns rise and fall times while driving a 1000 pF load with a 20 V square wave. This corresponds to a peak drive current of almost 1 A. In the amplifier circuit, with the output voltage swing set between 0 and 15 V, the gate capacitance of approximately 700 pF, and the same rise/fall times as in the above example, the circuit draws only 0.525 A. This is well within the maximum operating levels specified by the manufacturer.

Lastly, since the DS0026 was originally intended for functions such as RAM memory addressing, the output pulse width is logically controlled by the input pulse width; thus, the duty cycle information is preserved. In summary, the output of the DS0026 will be a 15 V square wave with the same duty cycle as the control signal. This output will drive the CMOS output stage, which is discussed next.

4.3.2.2 Output stage circuit

The output stage consists of complementary P-channel and N-channel power MOSFETs connected in a common drain configuration which specifies that the sources of the P-channel and the N-channel are tied to the high voltage supply (V^+) and ground, respectively.

The gates and drains of the two MOSFETs are tied together to form the input and output, respectively. See Figure 4.2. With the exception of the operating voltage, the stage's configuration and operation is almost identical to that of a CMOS inverter. As the input from the Gate Drive Circuit (V_{IN}) increases from 0 to 15 V, the N-channel MOSFET will turn on at V_{IN} greater than or equal to $V_{GSN(th)}$ (where $V_{GSN(th)}$ is the gate-to-source threshold voltage for the N-channel MOSFET) and the P-channel MOSFET will turn off at $(V_{SS} - V_{IN})$ less than or equal to $|V_{SGP(th)}|$ (where $V_{SGP(th)}$ is the source-to-gate threshold voltage for the P-channel MOSFET) causing the output to go low. The output will remain low and will pull current from the load until the input decreases from 15 to 0 V. The P-channel turns on at $(V_{SS} - V_{IN}) \geq |V_{SGP(th)}|$ and the N-channel turns off at $V_{IN} \leq V_{GSN(th)}$, forcing the output high and pushing current into the load. Therefore, the stage acts as a complementary push-pull amplifier.

Note also that the output stage merely switches the load between the V^+ and ground as dictated by its input. This switching mode configuration offers several advantages

1. When the load is switched to V_{SS} , it virtually sees an ideal voltage source since the MOSFETs output impedance is only 0.4Ω . This gives the amplifier a high driving current capability since the load can sink as much current as the power supply can deliver (within the maximum drain current limitations of the MOSFET). Upon switching to ground, the load will have a low impedance path to ground, allowing any of its remaining energy to be dissipated through the ground.

2. Although an NMOS switch has short fall times but long rise times, the symmetry of the circuit offers fast rise and fall times. The fast speed is a result of the simultaneous action of the MOSFETs; as the P-channel MOSFET is turning off, the N-Channel MOSFET turns on and vice versa. This, however, presents a problem during periods when both MOSFETs are on. It will be covered more thoroughly in the next section.
3. This configuration is useful when driving inductive loads such as a stray or lead inductance, since it utilizes the intrinsic Drain-Source (D-S) diodes as free-wheeling diodes. The main consideration when driving inductive loads is the voltage transients caused by breaking the flow of current through the inductor. For example, if the P-channel MOSFET has been turned on such that a current has been established from the power supply rail to ground, then the switching of the load to ground will cause this current to be interrupted. However, according to $V = L(di/dt)$, an instantaneous change in current requires an infinite voltage across the inductance. Since this is simply not possible, the voltage across the inductance abruptly increases and continues to do so until it can drive a current through the inductance. This voltage normally tends to exceed the breakdown voltage limits of the MOSFET, causing permanent damage to the device. However, this can be prevented by using the MOSFETs in the common drain configuration. If the N-channel MOSFET is on, then a load current will flow through it from the inductance to the ground; however,

when the N-channel MOSFET turns off, the current's path to ground will be blocked. Instead of causing a voltage transient, the current will flow through the P-channel's D-S diode into the positive supply rail. This diode channels the current away from the MOSFETs and clamps the flyback voltage to V^+ so that the complementary MOSFET is protected from the flyback voltage breakdown. It is readily apparent that this will also hold when the P-channel is initially conducting. The effectiveness of this means of suppression is contingent on whether the D-S diode can quickly and adequately clamp the flyback voltage. Since the diode has a comparable maximum current rating and switching speed with respect to its power MOSFET, it is normally adequate. However, should the need arise, a fast switching diode such as a Schottky diode could be placed in parallel with the D-S diode to shunt any excess current and protect the integral D-S diode.

4. This configuration draws very little quiescent current for both levels of input. The operating point of the output stage can be determined for either state of the input. For a high input, the operating point is simply the intersection of the I_D - V_{DS} characteristic curve for the N-channel MOSFET at $V_{GSN} = 15$ V and the I_D - V_{SD} curve for the P-channel when $V_{SGP} = 0$ V. To illustrate this, the characteristic curves of the two MOSFETs are shown in Figure 4.3. The intersection of the curves indicates the operating point. Although this is a qualitative estimate (since the $V_{GSN} = 15$ V curve and the

$V_{SGP} = 0$ V curve are not shown), it serves its purpose in representing how little current the MOSFETs will draw while still maintaining the required low output. The actual current will be lower since the curves' intersection and operating point will all be lower. For a low input, the operating point is given by the intersection of the I_D - V_{DS} characteristic curve for the N-channel MOSFET at a $V_{GSN} = 0$ V and the I_D - V_{SD} curve for a P-channel MOSFET with $V_{SGP} = 15$ V. According to the curves, given in Figure 4.4, the operating point will be at V_{DD} , still requiring very little quiescent current. Thus, the transient current dissipation is extremely small in both states. Note that this analysis will only hold if V_{SGP} is kept at 15 V. Therefore, if the P-channel MOSFET is operated at levels higher than 15 V, it becomes necessary to shift the gate's input voltage such that this relationship is maintained.

4.3.2.3 Level shifting circuit

The level shifting circuit allows the 0 to 15 V signal from the gate drive circuit to deactivate the P-channel power MOSFET. Since the P-channel source with a threshold voltage of $V_{SG(th)} = -2$ V is tied to V_{CC} through a source resistor, R_S , the P-channel FET will not turn off until

$$V_{SG} < V_{CC} - I_D R_S - 2 \quad (4.3)$$

where V_{SG} is the gate to source voltage, and I_D is the drain current. If I_D is assumed to be 0.2 A (the nominal current drawn by an amplifier when driving a transducer element in the Sector Vortex

Array with $R_S = 10 \Omega$ and $V_{CC} = 100 \text{ V}$), then the P-channel will remain activated until $V_{SG} = 96 \text{ V}$ or less. However, the maximum that the gate drive circuit will output is only 15 V , and thus the P-Channel FET will remain on continuously. In actuality, since the maximum V_{SG} that the P-channel MOSFET can withstand is only 20 V , the P-channel FET would probably experience a source-to-gate breakdown. In order to avoid this, the level shifting circuit elevates the output of the gate drive circuit to roughly $V_{CC} - 15 \text{ V}$ and feeds this into the P-channel FET. The output is elevated by setting the steady state voltage at the gate of the P-channel to be V_{CC} through a large pull-up resistor ($R = 100\text{K}\Omega$). In the absence of an input signal, there is no path for any current to flow; thus the resistor allows V_{SG} to settle at V_{CC} . The gate drive signal is then ac coupled into the gate voltage via a 4700 pF capacitor that presents a relatively low impedance to signals with frequencies as low as 500 kHz . This will effectively block the steady state voltage of the P-channel from reaching the N-channel. When the gate drive signal goes high, the ac coupled P-channel gate signal would swing to 115 V . However, this would limit the negative swing of the ac coupled signal to 100 V , which is insufficient to switch the P-channel FET. Thus, a clamping diode, in parallel with the pull-up resistor, is used to limit the maximum gate signal to 100.7 V (There is a 0.7 V drop to forward bias the diode.) Therefore, when the gate drive signal goes low, the ac coupled signal will drop to 85.7 V . This will cause the P-channel FET to go into the saturation mode without exposing it to voltages exceeding its gate to source

breakdown. Thus, the level shifting circuit offsets the ac coupled signal by 85.7 V in order to regulate the P-channel FET.

4.4 Hardware

Although the Hitachi 2-SK400 N-channel MOSFET and a 2-SJ114 P-channel MOSFET were used in initial amplifier prototypes, they subsequently were replaced by a Samsung IRFP-9230 P-channel MOSFET and a IRFP-230 N-channel MOSFET. The Samsung MOSFETs offer comparable performance at considerable cost reduction. For example, both the IRFP-9230 and the IRFP-230 have a maximum operating voltage of 200 V and a maximum drain current of 9 A. If they are used to drive a 50 Ω resistive load, the output power would be on the order of 800 W, which exceeds by far the nominal power needed to drive an individual element. The MOSFETs are operated below the maximum voltage to allow a margin for transients while still providing a large power output. Ceramic capacitors with their relatively low inductance were used for the 4700 pF capacitors; electrolytic capacitors with their small size were for the 10 μ F capacitors. The diode is a rectifier diode with fast switching speed and large current capability. Molded carbon resistors were used for the pull up and source resistors because of their relatively low inductance even at high frequencies. Although wire wound resistors offer higher power handling capabilities, their use is prohibited by their high inductances. Minimizing inductance is important because it can cause voltage spikes when presented with current spikes. These spikes will be largest during periods of simultaneous conduction. Also, resonant circuits, set up by inductances and

parasitic capacitances can cause ringing in the power supply rails and the grounds. Figure 4.5 shows the ringing at the amplifier output when the same size wire wound resistors and carbon resistors are used as the source resistors. This ringing can couple into the output of the gate drive through the ground and power supply rails. In turn, ringing on the gate drive output can couple across the input capacitance of the MOSFET to further increase the ringing of the amplifier output signal. (Recall that the amplifier, operating in the saturation mode, only responds to the logic state of the input signal. Thus, the only way that small input noise signal can pass through the MOSFET to the output is via capacitive coupling.

Because the input gate capacitance is quite large and the noise frequency is high, capacitive coupling will be prominent.)

Figure 4.6 shows the additional ringing present on the gate drive signal and contrasts it to the gate drive signal of the configuration utilizing the carbon resistors. This ringing should be avoided at all costs because it will degrade the output signal. Furthermore, MOSFET failure can occur if the ringing causes the output signal to exceed the maximum gate to source voltage. Thus, the carbon resistors were used in lieu of their lower power handling abilities. The amount of power dissipated in R_S however can be increased by paralleling these carbon resistors.

4.5 Practical Considerations and Future Recommendations

The only major shortcoming in this design is a problem that is inherent in all CMOS inverters: the simultaneous conduction of both MOSFETs that occurs during input transitions. The positive

transition causes the N-channel MOSFET to be turned on before the P-channel MOSFET is turned off; negative transition causes the P-channel MOSFET to be turned on before the N-channel MOSFET is turned off. The duration that both MOSFETs remain on during the positive transition is a function of the input waveform rise time as well as the N-channel turn-on time, T_{NON} , and the P-channel turn-off time, T_{POFF} . Let $T_{PVGS(th)}$ denote the time it takes the input to achieve the turn-on potential for the N-channel MOSFET and $T_{PVSG(th)}$ denote the time it takes the input to reach the turn-off threshold for the P-channel MOSFET then the duration of simultaneous conduction during the positive transition, T_{SCP} , is given by Equation (4.4):

$$T_{SCP} = (T_{POFF} + T_{PVSG(th)}) - (T_{NON} + T_{PVGS(th)}) \quad (4.4)$$

The period that both MOSFETs conduct during the negative transition of the input wave is dependent on its fall time in addition to the P-channel turn-on time, T_{PON} , and the N-channel turn-off time, T_{NOFF} . If $T_{NVSG(th)}$ represents the time required for the input to fall to the turn on threshold for the P-channel MOSFET and $T_{NVGS(th)}$ represents the time it takes for the input to realize the turn-off potential for the N-channel MOSFET then the period of simultaneous conduction during the negative transition, T_{SCN} , is given by Equation (4.5):

$$T_{SCN} = (T_{NOFF} + T_{NVGS(th)}) - (T_{PON} + T_{NVSG(th)}) \quad (4.5)$$

Using the rise and fall times of the gate driver (DS0026) output, $T_{NVGS(th)}$, $T_{NVSG(th)}$, $T_{PVGS(th)}$, and $T_{PVSG(th)}$ can be calculated. The values for T_{NON} , T_{NOFF} , T_{PON} , and T_{POFF} are given in the data sheets for the N-channel MOSFET (IRFP-230) and the P-channel MOSFET (IRFP-9230). Using these values, T_{SCP} and T_{SCN} were calculated to be approximately 98 ns and 33 ns, respectively. Thus,

the MOSFETs will both be conducting for a total of 131 ns during one period of the output. At a frequency of 700 kHz, 18% of the output period is spent in the simultaneous conduction mode, during which most of the current drains into the ground, causing a significant power loss. Moreover, the high currents associated with this mode cause substantial noise problems (as was mentioned in Chapter 3) and possibly MOSFET damages.

There are two viable methods for dealing with simultaneous conduction: utilizing current-limiting resistors to minimize the magnitude of the rush current (discussed in Chapter 3) and introducing a delay to the gate inputs to directly prevent the simultaneous conduction. It is evident from Equation (4.4) that T_{SCP} can be reduced to zero if the rightmost sum is increased by T_D so that the two sums are equal. Although T_{NON} is fixed, it is possible to increase $T_{PVGS(th)}$ by introducing a delay with a time constant equal to T_D to the input of the N-channel. A simple RC circuit with time constant, $\tau = T_D$, can be implemented using the input capacitance of the MOSFET and an external resistor. According to the N-channel MOSFETs data sheets, the input capacitance, C_{ISS} , is 800 pF. Thus, if a 122 Ω resistor is placed in series with the gate input, the input waveform will be delayed by 98 ns causing the N-channel MOSFET to switch on at the same instant as the P-channel is switched off. A slightly larger resistor should be used to ensure asynchronous switching by the MOSFETs. Unfortunately, the external resistor will also delay the N-channel from turning off, thus defeating its purpose. This can be overcome by inserting a diode in parallel with the resistor. See Figure 4.7. This will make the delays

unidirectional; the deactivation of the N-channel will not be delayed since the charge stored in the gate capacitance will flow through the diode rather than the resistor [13]. The same approach can be used to delay the P-channel from turning on before the N-channel turns off on the negative transition. Since this approach involves physically altering the PCB, the first method was used. However, it should be definitely utilized in any future designs.

A general consideration intrinsic to this amplifier and CMOS is that the inputs must never be left floating. This will raise the output of the amplifier to $V^+/2$, which will force both MOSFETs into saturation. The resulting rush current will eventually cause the MOSFETs to fail. Thus, provisions must be made such that the amplifier is always referenced to an input.

Specifically, some problems that are normally associated with this type of complementary push-pull amplifier have been accounted for in this design. First, protection against silicon controlled rectifier (SCR) latch-up has been incorporated in the circuit. This occurs when the input exceeds the V^+ of the amplifier, causing the input protection diode of the P-channel to be forward biased. The large current that flows through the diode causes the MOSFET to increase in temperature and latch-up so that correct operation can only be restored by turning off the power source for the amplifier. Should this current continue to flow through the diode, it will eventually lead to the destruction of the MOSFET. A preliminary inspection of the circuit indicates that this cannot occur in the amplifier circuit used in UPADS. The 4700 pF capacitor at the input of the P-channel MOSFET will block any dc input voltage from

reaching the gate of the P-channel and prevent SCR latch-up. Even if a transient or spike does pass through the capacitor, the clamping diode will kick in and help dissipate the current into V^+ .

In the past, short circuits at the output often caused by faulty cables connecting the array to the matching circuit were the major cause of MOSFET failure. Thus, short-circuit protection has been implemented by setting source resistance, R_S , such that the maximum current pulled through the MOSFET is below the maximum allowable drain current even at the maximum operating voltage. Although this does result in an increased power loss in R_S , amplifier reliability was gained. If a short-circuited output occurs in the present system, R_S should be able to withstand the additional power dissipation for a short duration to allow the operator to shut down the system. In the event of resistor failure, since the impedance normally becomes quite large, the MOSFET will be protected. Thus, the only repair necessary will be that of the source resistors, which are relatively inexpensive.

The circuit layout emphasized minimizing path inductances. For example, the path between the gate drive circuit and the input of the MOSFET gate was minimized and made as wide as possible. Power supply buses were also implemented in this fashion and ground planes were used wherever the circuit layout allowed.

From the noise problems considered in Chapter 3, it is obvious that the power and ground buses could still use some improvement. For example, potential differences of almost 2 V were found on different locations of the high voltage ground due to the inductance and large current transients present on the bus. Connecting this bus

to a ground plane in various locations by ground straps minimized this difference in potentials. In future designs, multilayered boards with layers dedicated to power distribution and grounding should be used. If this is not feasible, power distribution should be designed as a tree network so that a main power supply trunk branches to various areas of the PCB to minimize voltage potential differences on the bus.

Lastly, a form of output feedback is present in the circuit. As the drain current flows through R_S , a voltage drop proportional to this current occurs in series with the output voltage. In the event of large drain currents, this voltage drop will reduce the effective voltage between the gate and the source in the P-channel. Recall that as V_{SGP} is decreased, the MOSFET will come out of the saturation mode so that the drain current will subsequently decrease. Therefore, this negative feedback protects the MOSFET by shutting it down when large drain current is present.

Future modifications should include gate protection which can be implemented using a varistor or zener diode. For example, a 15 V zener diode placed across the gate-to-source inputs of both MOSFETs will prevent any input transients from causing a gate-to-source breakdown. Also, placing a resistor-capacitor (RC) snubber across the drain-to-source outputs will help to reduce any remaining ringing present at the outputs.

The culmination of these modifications and the decision to use the power MOSFETs as the output stage have led to an amplifier with many desirable characteristics: high resistance to electrical failure, minimal drive requirements, high operating temperature, fast

switching speeds, and a high power output capable of driving reactive loads. Through the combination of proper circuit layout, adequate decoupling, component selection, and effective modifications, this amplifier has a response that is comparable to commercial amplifiers. For comparison, the response of an amplifier taken from a Motorola data book is displayed in Figure 4.8. The MOSFET used in this amplifier has a comparable input capacitance, maximum operating voltage, and maximum drive current to the ones used in the UPADS' amplifier. Also, the gate drive used in this circuit is identical to the one used in the amplifier circuit. Figure 4.9 displays the response of the UPADS' amplifier operating at the same output levels utilizing identical inputs. The UPADS' amplifier output compares quite favorably to that of the Motorola amplifier. In conclusion, this amplifier should prove to be durable as well as capable of driving the loads presented by the phased array applicators.

CHAPTER 5

SYSTEM BUS IMPLEMENTATION

5.1 Design Objective

The system bus interconnects the individual components of the system. First of all, the bus provides a convenient means of directing power to the amplifier boards in the system. Secondly, all of the communication between the DMA and the amplifier boards is handled by the system bus. Finally, the output of each amplifier is connected to its corresponding matching network via the system bus. In Chapter 2, it was noted that this output could go as high as 100 V. At this high a voltage with frequencies ranging from 500 kHz to 1 MHz, it is very likely that there will be coupling between the high voltage amplifier signals and the low voltage DMA outputs as well as between the individual amplifier outputs. In order to prevent this, the high voltage signals were placed on a separate bus from the low voltage signals. This bus was specifically designed to reduce the crosstalk between these high voltage signals. The bus which carries the DMA outputs is designated as the low voltage bus and is designed to meet the standards of the IEEE P961 bus. In this chapter, the design and implementation of the low and high voltage buses will be discussed in detail.

5.2 Design Specifications

5.2.1 Low voltage bus

The low voltage bus (LVB) connects the amplifier boards to the interface board. In addition, the LVB has several important characteristics

1. The LVB should provide power to each board with power for the TTL circuits as well as the gate drivers used in the amplifier circuits.
2. The LVB should allow easy interconnection between the interface card and all of the amplifier boards in the system.
3. The LVB should be fully compatible with the IEEE standards.
4. The LVB should be card slot independent.

5.2.2 High voltage bus

The high voltage bus (HVB) links the individual amplifier circuits and their respective matching circuits. Since the maximum output voltage of each amplifier is almost 100 V, and the maximum drive current of each amplifier is approximately 9 A, the HVB must have a high power handling capability. Since this type of bus is rather uncommon in industry, it was necessary to design an in-house customized bus. Several important design specifications were considered in the design and implementation of the HVB

1. One of the HVB's duties is to distribute the high voltage that is required by all of the amplifiers. The power buses used to implement this supply should have a low impedance to minimize differences in potentials on the bus.

2. The main function of the HVB is to deliver the high voltage signals generated by the amplifiers to their corresponding matching circuits. These signals pass from the amplifiers to the matching circuits through an organized layout of parallel traces which makes the bus act as a controlled transmission line [14]. Unfortunately, transmission lines of this type cause crosstalk to occur between adjacent signals. This could lead to an appreciable degradation of the signal. Although it is practically impossible to entirely eliminate this type of interference, it is essential that the interference be reduced so that the distortion reaches an acceptable level.
3. If various phased arrays are to be driven using this system, their respective matching circuits must be readily interchanged.

5.3 Circuit Description

5.3.1 Low voltage bus

The LVB's main purpose is to connect the amplifier boards to the interface board. Recall that the DMA outputs the information from the interface board directly onto the bus. This information is then pulled off the bus using certain addressing hardware on the amplifier boards. Thus, this bus acts as an extremely important link between the DMA and the remainder of the system.

The main reason for using an IEEE standard bus is the availability of commercially supported hardware such as microprocessors and prefabricated backplanes. Also, because the

bus protocol has already been standardized, additional hardware and peripherals can be added to the system with very little difficulty. For example, if a microprocessor is needed to control a feedback system, it can be purchased completely configured.

Finally, card slot independence gives the system a modular design that makes the amplifier boards completely interchangeable. This allows rapid repair of a specific board by simply replacing it with another one. It only requires the proper address to be set on the replacement board.

From Chapter 2, it was noted that the system requires an eight bit data bus, and an eight bit address bus (including the load bit). Using the above criteria, the IEEE P961 STD bus was chosen because it has a separate eight bit data bus and eight bit address bus. Designed for use with microprocessors, the STD bus features interrupt requests, memory input/output (I/O) and an auxiliary power bus which can be used to power the gate drivers [15].

5.3.2 High voltage bus

First, it was necessary to implement the power bus for the amplifiers on the HVB which could tolerate voltages and currents far exceeding the specifications for the STD bus. Large currents require the impedance of the power bus to be minimum; otherwise, on the same power bus there may be spatial variations in the voltage potentials. This also applies to the ground bus (or ground planes) because large currents acting upon small impedances in the ground bus will elevate the ground potential. Since each amplifier is triggered with respect to ground, different ground potentials could

cause certain amplifiers to trigger prematurely. This, in turn, would severely corrupt the phase information of the signal. In order to minimize the impedance of the power bus on the PC board, the power distribution is made through thicker and wider traces. On the prototype HVB, the thickness of the copper clad is on the order of 0.0054 inch. Accordingly, the power buses are widened to about 0.15 inch. The ground bus impedance is also minimized by using ground planes wherever possible throughout the entire PC board.

Secondly, the bus should be designed such that the various distortion-causing factors are reduced as much as possible. Electromagnetic interference created by the amplifiers can be reduced somewhat by utilizing large ground planes which act as effective shields. Accounting for capacitive coupling is a bit more difficult since it can have many different origins. First, this capacitive type coupling is prominent on PC boards with dual layers. Since the glass epoxy behaves as a good dielectric, a veritable capacitor is formed by traces on the top and bottom of the PC board. Thus, high frequency signals on either the top or bottom trace can capacitively couple to the trace on the opposite side [16]. This can be avoided by jogging the traces back and forth along the entire bus so that there is little overlapping of the signal traces. Inductive coupling can occur as crosstalk between parallel traces on the same side of the PC board. It is most likely to occur in situations where the frequency and the amplitude of the signals are both large. Capacitive coupling and crosstalk can be reduced by

1. Moving the signals farther apart and thus reducing the capacitance between the signals. Recall that capacitance is

inversely proportional to the distance between the plates. Thus, by moving the plates (traces) farther apart, the capacitance and the respective coupling diminish. If this spacing is kept uniform, the capacitive coupling can also be predicted and thus controlled [17].

2. Moving the signals closer to a ground plane also reduces capacitive coupling to a large extent by minimizing the signal-to-ground capacitance. The ground plane absorbs the electrostatic fringing fields and reduces the effective capacitance. The ground plane is also useful for EMI rejection.
3. Crosstalk can also be reduced by shielding the signal lines on the HVB PC board by interlacing ground buses between them. These ground buses are tied into the ground plane in numerous areas, and thus provide a low inductance shield between the respective channels.

Thus by minimizing signal line capacitances, capacitive coupling can be reduced. It is important to also minimize the ground and power bus inductance in order to prevent any current spikes from causing voltage spikes on both the power supply and the ground. These current spikes will occur when a capacitive load is driven with a square wave. This will be discussed in Section 5.5.1.

Recall that the amplifier boards must interface with the HVB so that the outputs of the amplifiers can be passed to the matching circuit boards. It was desired that the matching boards are interchangeable so that various arrays could be driven. Therefore, each matching board has an edge connector that will mate with any

edge connector socket on the HVB. The HVB thus acts as a dual motherboard for the matching circuit boards and the amplifier boards.

5.4 Hardware

5.4.1 Low voltage bus

A Vector 4610-16 STD Bus 16 slot motherboard was used to implement the low voltage backplane. It uses a high quality glass epoxy printed circuit board (PCB), featuring a ground plane, full faraday shielding of all signal lines, and extensive decoupling for all power buses. Each amplifier board is designed with a built-in STD edge connector, which mates with the slots on the Vector motherboard. The amplifier boards, inserted in the first eight slots, are connected to the interface board which occupies the ninth slot.

5.4.2 High voltage bus

The hardware required for the construction of the HVB were

1. Printed circuit board generated by PCI from artwork generated by the Computer Aided Design (CAD) program smARTWORK using the criteria established above.
2. Eight Texas Instruments' one-hundred pin dual edge connectors.
3. Eight TRW fifty pin dual edge connectors.
4. One Kulka quick connect PC mount barrier strip.

The Texas Instruments (TI) connector features bifurcated contacts with gold plating for low contact resistance and high corrosion resistance. Bifurcated contacts feature two independently sprung

contacts for each finger for added reliability. The TRW connector features gold plated beryllium contacts with a large voltage and current handling capability. The Kulka quick connect PC mount barrier strip allows the HP6030A programmable system supply to be quickly connected to the HVB. The artwork generated by the CAD program smARTWORK is given in Figures 5.1 and 5.2.

5.5 Practical Considerations and Future Recommendations

5.5.1 Low voltage bus

There is a definite problem in driving a capacitive load with a square wave. According to the equation, $I = C(dV/dt)$, the current required to switch the voltage is proportional to the change in voltage over time and the capacitance. Since the change in voltage over time is already defined as the slope of the rising edge and falling edge of the square wave and is subsequently quite large, it is necessary to minimize the capacitance. However, in practice, it is impossible to realize a bus without any stray capacitance. The longer signal paths are normally accompanied by a larger wiring capacitance. Furthermore, this capacitance is supplemented with the input capacitances of the gates of all the integrated circuits on the bus. The typical input capacitance of a gate averages about 7.5 pF. In the case of the LVB, 8 gates are connected in parallel to each bus line for an input capacitance of approximately 60 pF. Although the voltage swings are relatively small (approximately 3 V) on the LVB, the transition times are extremely short. For example, the typical rise time, t_r , of a 74LS series chip is only 15 ns. The fall time, t_f , is even shorter, about 6 ns. Thus, the current

that must be sunk and sourced by an IC which outputs to the bus is 30 mA and 12 mA, respectively. Since this current is directly proportional to the capacitance, an additional capacitance presented by the bus will cause a subsequent increase in current. Also, the typical sink and source current of a LS74 series IC is only 16 mA and 3 mA, respectively. Thus, the typical LS74 series IC can not satisfy these high current drive requirements. Therefore, it was necessary to implement line drivers with high current sinking capability to drive these bus lines. Some 74LS244 octal tristate drivers were used to implement the bus drivers and are located on the interface card.

These bus drivers may cause additional problems. When the bus driver makes the transition from V_{OH} to V_{OL} , the drive current will be sunk for only a short duration, roughly equivalent to the transition time, and therefore forms a current spike. This current spike will travel along the ground line causing a voltage spike, as given by the equation, $V = L(di/dt)$, that is directly proportional to the inductance along its path. The inductance of the ground line is given by the length of the path multiplied by the average wiring inductance. Using an average wiring inductance of about 12.7 nH/inch, the bus presents an inductance of almost 152.4 nH. This inductance, when presented with a current spike with a magnitude of 30 mA over a duration of 0.6 ns, will give a voltage spike as large as 0.762 V. Thus, an input expecting an active low signal could, in effect, receive an undefined input since the maximum V_{IL} is 0.8 V. Any additional bus capacitance would just increase this voltage over the maximum V_{IL} . One possible solution

to this problem involves the use of bypass capacitors. Bypass capacitors, when placed between the power lines and ground bus, present a high impedance to low frequency signals, but a relatively low impedance to high frequency signals, since the impedance of a capacitor is inversely proportional to the frequency. Thus, any high frequency signals on the power supply and ground will be removed by this capacitor. Frequently placing these bypass capacitors over the entire span of the bus will shorten the effective path that a current spike can travel. Shortening the path length will, in turn, reduce its inductance, and thus cause smaller voltage spikes.

Lastly, there will always be some distortion of the signal, which is unavoidable. This is especially true for signals such as clocks which have characteristically short transition times and high frequencies. In order to maintain the integrity of the signals, receivers were used at the inputs of each board. This minimizes the degradation of the signal by shortening the length of the path that it must travel before it reaches another gate.

In conclusion, it is apparent that no matter how well a bus is designed there will always be some inherent considerations that should be taken into account. The capacitive loading of fast signals should be compensated by using high current bus drivers. Power line decoupling is essential to reduce the voltage spikes induced by ground and power line inductance. Signal degradation should be minimized by using driver and receiver ICs on both sides of the bus.

5.5.2 High voltage bus

There are some inherent tradeoffs that were considered when designing this bus. First, due to space limitations, the power supply is connected on one end of the HVB. However, if there is any inductance in the power bus of the HVB, there could be a substantial difference in potential from one end of the board to the other. Ideally, the power supply should be connected to the center of the power bus with possibly more than one connection to allow for an even distribution of power.

Secondly, in order to facilitate the power handling requirements, HVB signal lines were widened. However, this increases the signal-to-ground capacitance. (Recall that the signal-to-ground capacitance is proportional to the area of the traces.) Since this capacitance is driven with the square wave output from the amplifier, the same problem that was encountered on the LVB will also be present on the HVB. Although the transition times of the MOSFET amplifier is 6.6 times smaller than the TTL transition times, the amplitude of the voltage being switched is 33.3 times larger. Thus, if the bus capacitances are assumed to be equal, the drive current will be 5 times larger in the case of the HVB. Using the same inductance constant, this translates into a voltage spike of almost 3.81 V on the power and ground lines. Since the gate threshold voltage, V_{GS} , of the P-channel and the N-channel MOSFETs are -2 V and +2 V respectively, these spikes on the power and ground lines could actually turn on the two MOSFETs. Thus, extensive decoupling of the high voltage power lines is necessary. Since decoupling is most effective when it is done near the current spike

source, the bypass capacitors were placed as close as possible to the amplifiers.

Hence, it is evident that the signal-to-ground capacitance and the power and ground line inductance should be kept to a minimum. This can only be achieved through proper layout and construction of the HVB backplane. If this does not bring the voltage spikes to an acceptable level, power line decoupling should be incorporated to prevent false triggering of the amplifiers by voltage spikes. In future designs, a multilayered board with separate layers for power planes, ground planes, and signal lines would provide the most effective means of reducing the parasitic capacitance as well as giving improved shielding for reduced crosstalk.

CHAPTER 6

THE SECTOR VORTEX PHASED-ARRAY

6.1 Introduction

Phased-arrays control the placement of the desired focus by driving a number of elements in a set configuration with specified phases and amplitudes. Using techniques such as the Pseudoinverse Pattern Synthesis Method, [18] the amplitude and phase information of each element's driving signal can be determined. However, should the phase shift and the efficiency of each element differ, the actual amplitudes and phases of the pressures generated by the elements would also deviate from their expected values, producing changes in the synthesized acoustic field pattern of the arrays. Thus, variations between different elements' efficiencies and phases must be quantized and compensated. The most efficient method, which is currently being studied, is to account for such variations in the actual derivation of the excitation signals. The other alternatives involve either corrections in the software used to generate the presets of the counters, or a hardware implementation which actually modifies the driving signal using passive networks. The software correction allows a simple means for compensating for such deviations, but may be limited by the resolution of the system. Recall that the phase resolution is 22.5° and the amplitude resolution is a 6.25% duty cycle. A hardware implementation, incorporated in the matching network, affords a higher resolution that is limited only by the actual measurements of these deviations.

A design for a matching network which accounts for differences in efficiencies and phase shifts has been developed. Although the matching networks have a general form, they are designed specifically for each element according to their driving characteristics. In order to evaluate the performance of the matching network and UPADS, this design was applied to the piezoelectric transducer elements in the Sector Vortex phased-array. A brief description of this array follows, along with an in-depth discussion of the measurements involved in characterizing the elements.

6.2 The Sector Vortex Phased-Array

6.2.1 Array geometry

The Sector Vortex array consists of thirty-two elements mounted on a semi-spherical aluminum shell. The convex surface of the shell is mapped into two concentric tracks, with each track subdivided into 16 sectors. (See Figure 6.1.) Each sector is designated by a trapezoidal facet which is a flat surface that allows the transducer element to be mounted on the shell. There is a void inside the inner track of the shell, where a small diagnostic array might be placed in order to image the placement of thermocouples.

6.2.2 Construction

The transducer elements are trapezoidal in shape and are cut from rectangular slabs of PZT-4 using a diamond saw and a special rotating mount designed for this purpose. The elements are bonded to the shell described in the above section, using a conducting

adhesive which facilitated the bonding of the elements to the non-planer surface by requiring no compressive loading. Special shims were designed to allow an air gap between adjacent elements which will reduce mechanical coupling.

The surfaces of the PZT-4 have a layer of gold over a layer of chromium which serves as the electrodes. Electrical connection to each element's electrodes is made by a spring loaded contact which consists of a modified Subminiature Coaxial Connector (SMB) bulkhead jack and a brass contact. The brass contacts are all machined to a hemispherical surface with the same specifications and are mounted perpendicular to the face of the elements by pieces of spring steel attached to a circular mount. These contacts are normally gold-plated to prevent corrosion that may occur; however, since the array was constructed as a prototype, this was economically unfeasible. The point of contact between the element and the connector is on the center of the element to allow uniform current flow from the contact across the silver electrode. This interconnection configuration accomplishes several objectives

1. The area of contact between the element and the electrical connector will be consistent from one element to another.
2. The mechanical perturbation introduced by the contact will be the same for each element.
3. The power distribution produced by the electrical connector will be even and uniform among various elements.
4. Vibration in each transducer will be accommodated by the give in the spring mounting of the contact.

Coaxial cables (RG-174) are used to connect the contacts to the driving system to facilitate disassembly from the SMB bulkhead jacks.

The shell provides the ground node for the electrical connections. It will also act as a quarter wave-matching layer since its thickness is approximately one fourth of the wavelength of sound in aluminum at the given operating frequency, and the acoustical impedance of the aluminum is roughly the geometric mean of that of the piezoelectric ceramic and the water. Thus, the shell will theoretically act as an acoustical step-down transformer that allows perfect transmission of the ultrasound waves into the water.

The transducer and shell apparatus is then enclosed in a water-tight housing with only the concave side of the matching layer exposed. The housing can be readily disassembled should the elements or the interconnects ever need servicing. The coaxial cables exit the housing through acrylic tubes that incorporate a strain release for each coaxial cable as well as an air tube which can be used to circulate air for element cooling if necessary [19]. Lastly, a beveled stainless steel shaft is provided for mounting the phased array applicator.

6.3 Characterization of the Sector Vortex Elements

In order to design the matching circuits for the Sector Vortex Array, each element in the phased-array must be characterized by analyzing its various responses. Utilizing this information, the matching circuits are then designed at an optimum operating frequency to

1. Normalize the output of each element so that there will be equal acoustical pressure contribution by all of the transducers in the array.
2. Normalize the phase shifts introduced by each element to minimize the variation in the phases of the pressure generated by different elements.

This is particularly important in the Sector Vortex phased-array which utilizes the interference between patterns synthesized by the inner and outer track elements to control its annular focus [20].

6.3.1 Determining the operating frequency

The frequency response of an element is determined by measuring the acoustical pressure generated by the element as the driving signal frequency is varied. Although a variation is expected between the elements in different tracks due to the difference in size, there actually was a large deviation between elements of the same size. Compared to the smaller elements on the inner track, the larger elements on the outer track had less deviation between their frequency response and also a more defined single resonance point instead of multiple resonances. More importantly, the output pressure of the smaller elements were significantly lower than the larger elements. For the sake of comparison, the frequency responses of each track and the entire array were measured. From these plots, it was apparent that the frequency response of the entire array is dominated by the outer track elements with the inner track contributing only about one third of the pressure generated by the outer track. Thus, the inner track may not be instrumental in

synthesizing a field pattern and the Sector Vortex array may be acting as a one track applicator. This could compromise the performance of the array because additional tracks allow a larger focal annuli to be synthesized and better control of power deposition patterns in the depth direction [21]. Also, further control of the However, for optimal operation of the Sector Vortex array, this contribution should be equal which requires either the output of the inner track elements to increase or the output of the outer track elements to decrease. The acoustical pressure of different elements was measured as the voltage of the driving signal was increased. It was found that comparable pressures could be generated at subsequently high voltages, when an element was driven at its resonance frequency. Unfortunately, as is obvious from the frequency responses of the elements, the resonant frequencies of the elements are not the same; even the large elements have small deviations in their resonant frequencies. This constitutes a problem because the driving system can only be operated at one specific frequency. Thus, although the resonant frequencies may differ by only a few kHz, it is the magnitude of their responses at a particular frequency that is relevant. This problem is compounded by the difference in the average resonant frequency between tracks and the high Q of these responses. Thus, a particular element cannot be driven at its resonant frequency without driving other elements off resonance and subsequently sacrificing their efficiency. Thus, in order to ensure equal contribution from all of the elements, the operating frequency was chosen between the average resonant

frequencies of both tracks. The guidelines used in making the selection are given below:

1. The output of each element at this frequency should be as close as possible to its maximum output in order to maintain some level of efficiency.
2. The variations in the output of the elements in the array should be minimal at this frequency.
3. Since the outer track constitutes the major source of power in the array, its elements weigh more in the frequency selection.

Using these guidelines, the optimum operating frequency was determined to be 708 kHz.

6.3.2 Determining the normalized acoustic pressure

The next step is to determine the maximum possible pressure that still falls within the acoustic output range of *each* element in the array at the optimum frequency. This was accomplished by measuring the acoustic pressure generated by an element as the driving signal voltage was incremented. The applied voltage for the outer track elements was limited to a maximum of 50 V since most of the elements achieved a significant pressure level in this range; the elements in the inner track were driven up to 100 V to compensate for their low efficiencies. A hydrophone was used to measure the pressure generated by each element. The pressure is thus given in terms of the output voltage of the hydrophone. By examining the plots for the maximum V_{rms}^2 that is attainable by all of the elements and the respective applied voltage, V_{AI} , that is

required by the l^{th} element, gives the maximum normalized pressure, P_{max} . In other words, if each element is driven with their respective applied voltage, they will generate the same acoustic pressure, P_{max} . Using the applied voltages required to achieve this pressure and the impedance of each element measured by a HP4193A Vector Impedance meter, the power delivered to the elements can be calculated. This corresponds to the power that is required by the specific element, to generate the normalized pressure, P_{max} .

6.3.3 Phase measurements of the individual elements

Lastly, the phase of the acoustic pressure relative to the driving signal of each element was measured. This was accomplished by placing the hydrophone at the geometric focus of the array, and driving each element individually. The output of the hydrophone was then cross correlated with the driving signal since the interval between the maximum of the cross correlation and its origin can be related to the phase difference between the two input signals by the relation

$$\Phi = (360^\circ)f_0t \quad (6.1)$$

where f_0 denotes the operating frequency, t denotes the time delay, and Φ represents the phase shift. The total phase difference consists of

1. The time delay required by the acoustic wave to traverse the distance from the element to the hydrophone.
2. The phase shift introduced by the element.

Since the hydrophone is placed in the geometric focus of the array, the phase shift due to the acoustic path length will be equal. Thus, the former can be considered irrelevant. Thus, the total measured phase difference can be related to the phase shift introduced by the elements. The device used to digitize the input signal and perform the cross correlation was a Data Precision D6100 Universal Waveform Analyzer. Since its sampling rate is 50 MHz, the maximum resolution of the phase shift measurement is approximately 5° . As a side note, the magnitude of the cross correlation function is related to the ratio of the signal from the hydrophone and the driving signal. Thus, in theory, this information could be used as the scaling factor for the magnitude of the element's output. In practice, however, since each element's impedance varies, the amplitude of the driving signal will vary also. Unless the amplitude of the driving signal is compensated, the amplitude of the cross correlation will give an incorrect scaling factor [22].

CHAPTER 7

MATCHING CIRCUITS

7.1 Design Objective

The matching circuits are two port networks which transform the complex impedance of the elements to resistive loads which will be driven by the amplifiers. Since they are constructed completely out of reactive components, there theoretically should be no power dissipated in the circuits. In practice, there is probably some power losses due to some resistive components in the inductors and core losses in the toroids used to implement them. From the discussion on the Sector Vortex phased array in Chapter 6, it is apparent that there are three essential requirements for its optimal operation:

1. A given duty cycle should effect the same acoustic pressure from each element in the array.
2. A given phase shift from the DCC should generate an identical phase shift in the acoustic pressure from all of the elements in the array.
3. The reactance of the load driven by the amplifier should be reduced in order to maximize the real power delivered to the element.

The main objective of the matching circuit is to compensate for the large variations in efficiency and phase angle between different elements which could drastically alter the actual driving signals from the desired ones, as discussed in Chapter 6. The input

parameters for each element's respective matching network were determined through the individual characterization of the individual element. These parameters are listed below:

1. The optimal frequency, f_0 , for equal acoustic pressure from all of the elements in the array.
2. The electrical impedance of the element at f_0 .
3. The voltage required by the element to generate the normalized acoustic pressure at f_0 .
4. The characteristic phase shift introduced by the element at f_0 .

Utilizing these parameters, the matching networks can be designed to satisfy the requirements for optimal operation.

7.2 Design Specifications

For a better understanding of the design problem, a simple model of the electrical impedance of a piezoelectric transducer is presented. Although better models such as the KLM model use a distributed element approach of transmission line theory, a lumped element model should suffice for this particular application since the elements will be driven only at a frequency near resonance. The frequencies at which the elements are relatively efficient are restricted. The respective interaction of the parameters can be modeled by an equivalent network to approximate the element's electrical impedance (See Figure 7.1.) Each of these parameters is analogous to a mechanical characteristic of the transducer: C_1 is the effective mechanical capacitance related to the stiffness of the

crystal; C_2 is the capacitance of the transducer since it is virtually a capacitor with the electrodes and the ceramic material acting as the plates and the dielectric, respectively; C_3 represents any capacitance that might be introduced by the mounting and the electrical connection of the element; R is the resistance due to the radiation impedance and any internal losses in the transducer; L is inductance associated with the mass of the crystal [23].

When the excitation signal is at the resonant frequency, ω_0 , as defined by Equation (7.1)

$$\omega_0^2 = (1/LC_1) \quad (7.1)$$

the total impedance of the L and C_1 components in the series branch of the network will go to zero. Since conducting epoxy was used to bond the element to the matching layer, C_3 is fairly small and can be considered negligible. The network will thus reduce to a circuit with R and C_2 in parallel as shown in Figure 7.2. The power factor of this parallel network is fairly small and is given by Equation (7.2)

$$\cos(\Phi) = (1 + (\omega_0^2 C_2^2 R^2))^{-.5} \quad (7.2)$$

where Φ denotes the phase difference between the total current in the transducer, I_T , and the current in the resistor, I_R . The small power factor indicates that only a small portion of the total power is being transmitted to and dissipated by R in the form of real power (electrical power that is actually converted to mechanical power) causing very little power to be radiated from the transducer [24]. Thus, in order to maximize the real power, the capacitance C_2 must be tuned out. Using a simple transformation, these elements can be represented as a series combination as in Figure 7.3. Thus, this

capacitance can be cancelled with a series inductor, L_S , given by Equation (7.3).

$$L_S = (1/\omega^2 C_2) \quad (7.3)$$

to present a real load to the amplifier.

It is important to note that although the current may be in phase with the voltage when it enters the element/tuning inductor combination, there will still be a phase shift as it enters the element introduced by the element's complex impedance. From the model given above, the reactance of the element will be dominated by the parallel capacitance, C_2 , at the resonant frequency, causing the current to lead the voltage by this phase angle. The resulting instantaneous power leads the instantaneous power that would be generated without phase shift by one half of the phase angle between the voltage and current. Therefore, if the time $t=0$ is taken as a reference, then it appears that the instantaneous power produced by the out-of-phase signals is delayed with respect to the power given by the in phase signals.

The instantaneous acoustic power radiated by the element is proportional to the instantaneous electrical power delivered to it. Since the acoustic pressure generated by the element is directly related to its instantaneous acoustic power, a phase shift in the instantaneous electrical power will in turn cause a phase shift of the acoustic pressure with respect to its driving signal. Part of the phase shift between the element's driving signal and the output signal of the hydrophone must be attributed to the time delay required for the sound wave to propagate from the element to the hydrophone. However, if the hydrophone is placed in the geometric

focus of the array, the acoustic path length, and subsequently, the respective phase shift, should be identical for each element since the medium is homogeneous. Thus, the relative phase shift will be entirely due to the respective element and its interconnections. Since the speed of the electrical current is several orders of magnitude larger than the speed of sound, any variations due to contact and cable length should be negligible. The main source of error occurs because it is impossible to simultaneously drive all of the elements at their resonant frequencies. Thus, the reactance of the elements operating off-resonance cannot be solely caused by the parallel capacitance but also to the phase shift by the other elements in the network. For all practical purposes, the phase shift can be attributed to the effect of the each element's reactances on the phase angle between the applied voltage and the current. The variation in the phase angles of different elements was established in Chapter 6.

To ensure the desired phase outputs generated by the elements, it is necessary to counter the phase shift introduced by each element and subsequently normalize the phases of all the elements' acoustic pressure. Compensation of phase shifts can be accomplished either in the software used to create the excitation signals or in the hardware. The software version could utilize a look-up table with the measured phase correction for each element. A hardware implementation for phase correction would involve pre-phase shifting the current of the output signal by the phase angle *previous* to driving the element since the phase shift is related to the phase angle between the voltage and the current. Both

implementations are limited by the accuracy of the phase difference measurement. However, the phase correction resolution for the software system is limited to the phase resolution of the system, which is 22.5° . The phase resolution of the hardware implementation is theoretically unlimited because any specific phase shift is possible. In reality, this phase shift correction is a function of the availability and the precision of the required components. Because the hardware system offers higher resolution for phase shift correction, it is incorporated in the matching circuit.

In order to ensure a uniform amplitude response among the elements (a specified duty cycle will effect the same acoustic pressure from each element) there must be compensation for the efficiency variation. This may be accomplished by the impedance transformation. In this case, conventional matching of the load impedance to the source impedance is not feasible because the source impedance is extremely small. Even at low voltages and despite maximum power transfer, this would still result in a tremendous amount of power being dissipated within the amplifier which would drastically decrease the power conversion efficiency. On the other hand, impedance transformation can be used as a means of increasing the power transmitted to a particular element which will subsequently increase its acoustic pressure output. Since the amplifiers are being operated well within their bounds, they will act as a constant voltage source. Therefore, the output power of the amplifier is the time average of the square of its voltage divided by its load impedance (assuming a real load.) Thus, by applying the impedance transformation so that the input impedance of the

matching circuit/element combination is lower than the original impedance, the input power to the element can be increased. Besides, since the matching network consists of only reactive components, there will be no power lost in this network; thus the increased input power will be present at the inputs of the elements.

From the plots in Chapter 6 of the acoustic pressure output of each element with respect to applied voltage, the maximum acoustic pressure that could be achieved by all 32 elements at the specified frequency was determined. Using the impedances of the elements that were measured in Chapter 6 and the corresponding voltages needed to generate the maximum pressure for each element, the total average power delivered to each element can be calculated. The total average power delivered to each element, P_D , is given by Equation (7.4):

$$P_D = V_{rms}^2 / R \quad (7.4)$$

where R denotes the real impedance of the element. Since the output of the amplifiers is a square wave with a maximum equal to the applied voltage V_A , a minimum voltage equal to 0 V, and a 50% duty cycle, the rms value, V_{rms} , is given by Equation (7.5)

$$V_{rms} = ((V_A^2 T_{ON})/T)^{.5} = V_A/(2)^{.5} \quad (7.5)$$

where T_{ON} denotes the duration when the voltage is at V_A , and T denotes the period of the square wave. However, the output of the matching circuit is a sine wave, the rms value of the voltage, V_{sinrms} , is given by Equation (7.6)

$$V_{sinrms} = V_{o-p}/(2)^{.5} \quad (7.6)$$

The impedance required to produce the normalized acoustic pressure, R_N , for a system operating voltage, is given by Equation (7.7)

$$R_N = R (V_{\text{sinrms}}/V_{\text{rms}})^2 \quad (7.7)$$

Thus, each matching circuit can be used to compensate for variations in efficiencies by controlling the average power delivered to its respective element using the impedance transformation.

In summary, in order to implement the design objectives, the matching circuits must be capable of

1. Cancelling the reactive component of the element.
2. Introducing a phase shift to the driving signal current with respect to the applied voltage.
3. Transforming the impedance of the element such that the average power delivered to the element causes it to generate the normalized acoustic pressure.

The next section derives the network used for the matching circuit.

7.3 Circuit Description

The circuit used to implement the matching circuit is a 2-port, 4-terminal, asymmetrical T-network with an element in each of its branches, Z_1, Z_2, Z_3 . (See Figure 7.4.) Its purpose is to transform the impedance of the element, R_E , to the normalized impedance, R_N , while introducing a phase shift, Φ . The image impedances of an asymmetrical network are the impedances Z_A and Z_B such that if Z_A (Z_B) is placed at the output (input) of the network, the impedance looking into the input (output) will be Z_B (Z_A) [25]. The image impedance for the T-network is defined in this way:

If R_N is placed at the input of port 1, the input impedance at port 2 must be R_E where R_E is given by,

$$R_E = Z_2 + ((Z_1 + R_N)/(Z_1 + Z_3 + R_N)) \quad (7.8)$$

If R_E is placed at the input of port 2, the input impedance at port 1 should be R_N where R_N is given by

$$R_N = Z_1 + ((Z_2 + R_E)/(Z_2 + Z_3 + R_E)) \quad (7.9)$$

Solving the 2 equations simultaneously for R_E and R_N in terms of Z_1 , Z_2 and Z_3 , gives

$$R_N = (A (Z_1 + Z_3)/(Z_2 + Z_3))^{.5} \quad (7.10)$$

$$R_E = (A(Z_2 + Z_3)/(Z_1 + Z_3))^{.5} \quad (7.11)$$

where A is given by

$$A = Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3 \quad (7.12)$$

The input impedance at port 1 with an open circuit at port 2 is given by Z_{O1} :

$$Z_{O1} = Z_1 + Z_3 \quad (7.13)$$

The input impedance at port 1 with a short circuit at port 2 is given by Z_{S1} :

$$Z_{S1} = Z_1 + ((Z_2 Z_3)/(Z_2 + Z_3)) \quad (7.14)$$

The input impedance at port 2 with an open circuit at port 1 is given by Z_{O2} :

$$Z_{O2} = Z_2 + Z_3 \quad (7.15)$$

The input impedance at port 2 with a short circuit at port 1 is given by Z_{S2} :

$$Z_{S2} = Z_2 + ((Z_1 Z_3)/(Z_1 + Z_3)) \quad (7.16)$$

Thus, Equations (7.7) and (7.8) can be replaced by

$$R_N = (Z_{O1} Z_{S1})^{.5} \quad (7.17)$$

$$R_E = (Z_{O2} Z_{S2})^{.5} \quad (7.18)$$

The equivalent circuit of the amplifier output, matching circuit, and the element impedance therefore can be represented as in Figure 7.5,

where V_1 and I_1 are the voltage and current at port 1, respectively and V_2 and I_2 are the voltage and current at port 2, respectively.

The image transfer constant, Θ , is defined by

$$e^{\Theta} = ((V_1 I_1)/(V_2 I_2))^{.5} \quad (7.19)$$

and Θ is complex

$$\Theta = \alpha + j\Phi \quad (7.20)$$

where α is the loss factor and the Φ is the phase shift. If the T-network is terminated by its image impedances, the voltage ratio is given by

$$V_1/V_2 = (I_1 R_N)/(I_2 R_E) \quad (7.21)$$

Substituting this into Equation (7.19) gives

$$e^{\Theta} = (I_1/I_2)(R_N/R_E)^{.5} \quad (7.22)$$

In order to solve for Θ , the right side of Equation (7.22) must be found. The ratio of I_1 and I_2 can be found using a current mesh analysis of the equivalent circuit and is given by

$$I_1/I_2 = (Z_{O2} + R_E)/Z_3 \quad (7.23)$$

The ratio of R_N and R_E can be found from Equations (7.17) and (7.18) and is given by

$$R_N/R_E = (Z_1 + Z_3)/(Z_2 + Z_3) \quad (7.24)$$

Using Equations (7.13) and (7.15), this reduces to

$$R_N/R_E = Z_{O1}/Z_{O2} \quad (7.25)$$

Thus, substituting Equations (7.25) and (7.23) into Equation (7.22) gives

$$e^{\Theta} = ((Z_{O2} + R_E)/Z_3)(Z_{O1}/Z_{O2})^{.5} \quad (7.26)$$

In order to generate an expression for Θ , the formula for the hyperbolic cosine and the hyperbolic sine was used. For example,

$$\sinh(\Theta) = (e^{\Theta} - e^{-\Theta})/2 = (1/Z_3)(R_N R_E)^{.5} \quad (7.27)$$

The expression for the hyperbolic sine was then divided into the expression for the hyperbolic cosine to get an expression for the hyperbolic tangent. After much algebra, this expression reduces to

$$\tanh(\Theta) = ((R_N R_E)/(Z_{O1} Z_{O2}))^{.5} \quad (7.28)$$

Multiplying Equation (7.28) by Z_{O1} and using Equation (7.25) gives

$$\tanh(\Theta) = (R_N/Z_{O1}) \quad (7.29)$$

Using Equation (7.13), this can be rewritten as

$$\tanh(\Theta) = (R_N/(Z_1 + Z_3)) \quad (7.30)$$

Substituting Equation (7.14) and Equation (7.17) into the above expression gives the $\tanh(\Theta)$ in terms of the elements in the T-network:

$$\tanh(\Theta) = (((Z_1 + (Z_2 Z_3))/((Z_2 + Z_3)(Z_1 + Z_3))))^{.5} \quad (7.31)$$

Lastly, each of the elements in the T-network must be solved. For example, Z_3 can be determined from Equation (7.27).

$$Z_3 = (1/\sinh(\Theta))(R_N R_E)^{.5} \quad (7.32)$$

Element Z_1 can be found by multiplying Equation (7.28) by Z_{O1} and using Equations (7.25) and (7.13)

$$Z_1 + Z_3 = R_N/\tanh(\Theta) \quad (7.33)$$

where Z_3 is given in Equation (7.29).

Impedance Z_2 can be found by multiplying Equation (7.28) by Z_{O2} and using Equations (7.25) and (7.15).

$$Z_2 + Z_3 = R_E/\tanh(\Theta) \quad (7.34)$$

Using Equation (7.29), the expressions for Z_1 and Z_2 are given in Equations (7.35) and (7.36), respectively.

$$Z_1 = R_N/\tanh(\Theta) - (R_N R_E)^{.5}/\sinh(\Theta) \quad (7.35)$$

$$Z_2 = R_E/\tanh(\Theta) - (R_N R_E)^{.5}/\sinh(\Theta) \quad (7.36)$$

Since the network is designed to be lossless, Z_1 , Z_2 , and Z_3 , must all be reactive. Replacing Z_1 , Z_2 , and Z_3 with jX_1 , jX_2 , and jX_3 , respectively, and substituting them into Equation (7.30) gives

$$\tanh(\Theta) = R_N/j(X_1 + X_3) \quad (7.37)$$

Equation (7.37) states that the $\tanh(\Theta)$ is imaginary. However, in order for the hyperbolic tangent to be imaginary its argument, Θ , must be imaginary. According to Equation (7.20), $\Theta = \alpha + j\Phi$. Therefore, in order for Equation (7.37) to hold, α must be equal to 0 and Θ must be equal to $j\Phi$. Using the hyperbolic trigonometric identities,

$$\sinh(j\Phi) = j\sin(\Phi) \quad (7.38)$$

$$\tanh(j\Phi) = j\tan(\Phi) \quad (7.39)$$

and substituting the reactances jX_1 , jX_2 , and jX_3 into Equations (7.35), (7.36), and (7.32) gives the reactance of each element in the network.

$$X_1 = -R_N/\tan(\Phi) + (R_N R_E)^{.5}/\sin(\Phi) \quad (7.40)$$

$$X_2 = -R_E/\tan(\Phi) + (R_N R_E)^{.5}/\sin(\Phi) \quad (7.41)$$

$$X_3 = -(R_N R_E)^{.5}/\sin(\Phi) \quad (7.42)$$

The sign in the above equations indicates the type of reactance necessary. A negative sign indicates that a capacitor is to be used to implement the reactance, and a positive sign represents that an inductor is necessary. Therefore, the components of the matching network can be selected by using the above equations, the measured R_E and Φ , and the calculated R_N [26].

7.3.1 Hardware

The hardware used to implement the matching circuits is listed below:

1. A matching circuit PCB.
2. TDK toroidal cores.
3. Ceramic or mica capacitors.
4. Pasternack right angle SMB jack.
5. Variable capacitors.

The matching circuit PCBs were designed by using smARTWORK. They feature a full ground plane on the component side of the PCB, an edge connector which mates into the HVB, and interleaved signal and ground traces on the solder side. As an added protection against crosstalk, a ground shield line, connected to the ground plane in numerous locations, was placed in between the pairs of signal paths and ground paths.

The TDK toroidal cores are used to implement the inductors because these cores' relatively high permeability allows large inductors to be made with relatively few turns. Although this compromises the resolution of the inductors, they can be supplemented with RF variable chokes if necessary. The cores are made out of a ferrite material, which gives it a good frequency response (up to 8 MHz) with relatively low power loss. The toroid's shape allows it to be self-shielding against crosstalk between channels since no lines of flux emanate from the core.

The capacitors used in the matching circuit have either a ceramic or mica dielectric. The mica capacitors have an excellent

frequency response with very little leakage current. The ceramic capacitors offer a fair frequency response with a good size capacitance in a relatively small package. Both will operate at high voltages and have good tolerances.

The right angle connectors mounted at the end of the matching circuit boards provide the final link between the UPADS system and the phased array to facilitate the connection of the cables of the phased arrays. Since it is an SMB type connector, it offers coaxial connections in a miniature package.

Finally, the variable capacitors can be used to account for variations in the cable capacitance. They are also mounted at the edge of the matching circuit board, which allows final adjustment of the matching circuits while the system is operational.

7.4 Practical Considerations

In order to minimize calculations, a program was written that calculates the reactances needed to implement the matching circuits using the inputted parameters in the given equations. In the case of an inductive reactance, it will also calculate the number of windings that is needed on the toroid in order to implement the inductor.

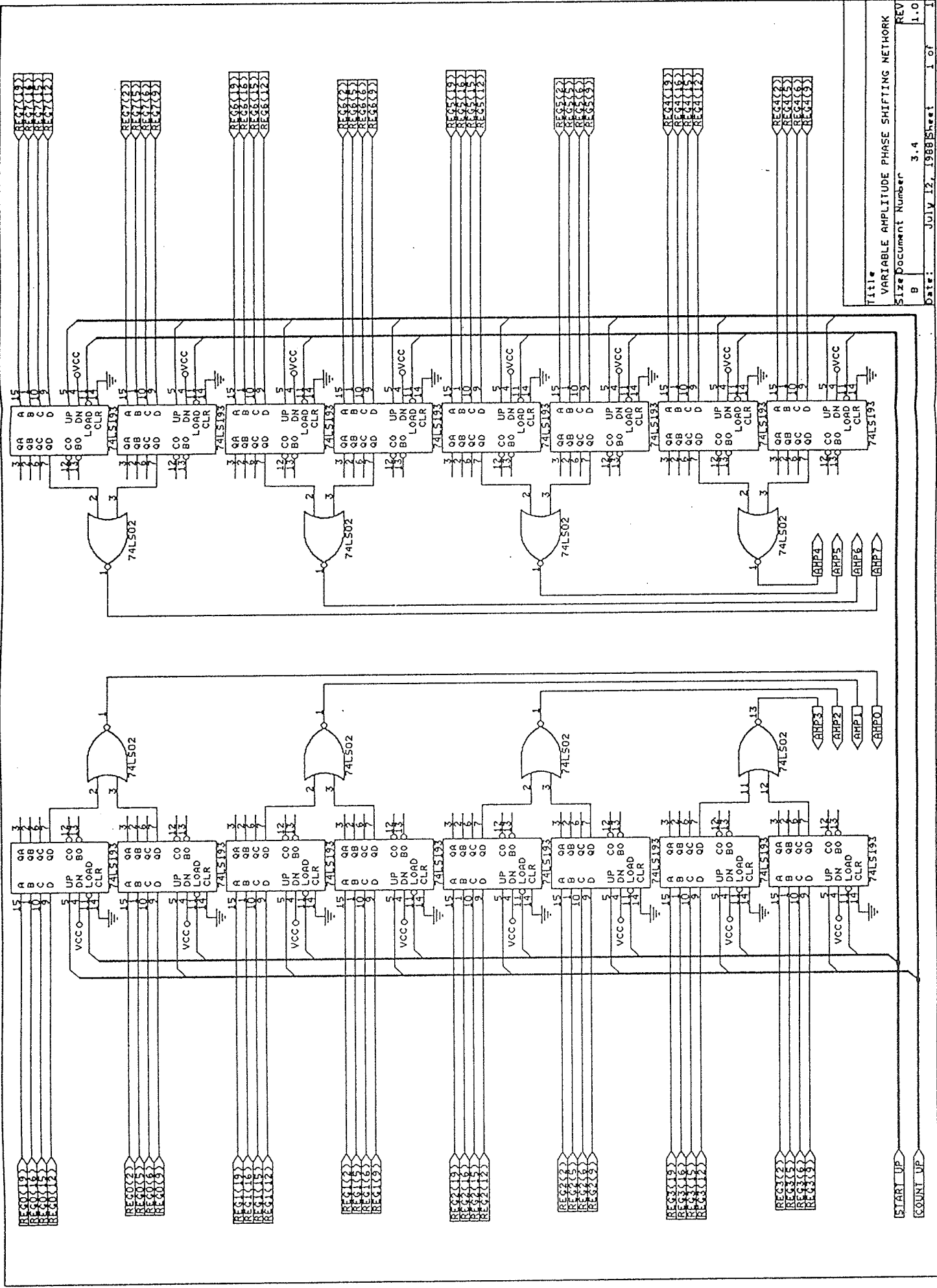
An effort was made to accurately realize the values given by the program. If a desired capacitance was not available commercially, several capacitors were paralleled in order to implement it. The toroids were wrapped with uniform spacing

between the windings to ensure that the magnetic flux lines were as uniform as possible.

CHAPTER 8

CONCLUSIONS

The main objective of the Ultrasonic Phased Array Driver System (UPADS) was to generate the desired excitation signals for all of the elements in a phased array. As a laboratory prototype, the system performed its task well. However, an ultrasound phased array system must incorporate some type of feedback in order to protect the patient as well as utilize phased-arrays to their fullest extent. While UPADS proved fairly successful as a phased-array driver, there were no provisions for any feedback. Acceptance into the clinic precludes a means of thermometry and system regulation. Further research is needed in this area.



Title: VARIABLE AMPLITUDE PHASE SHIFTING NETWORK
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Figure 2.1 The Variable Amplitude Phase Shifting Network

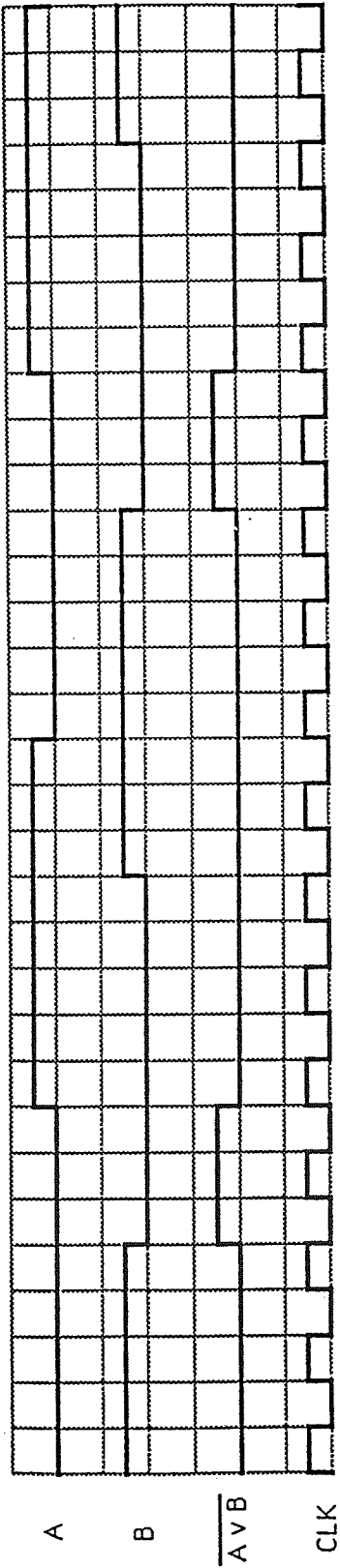


Figure 3.2. Implementing a Square Wave with a 18.75% Duty Cycle

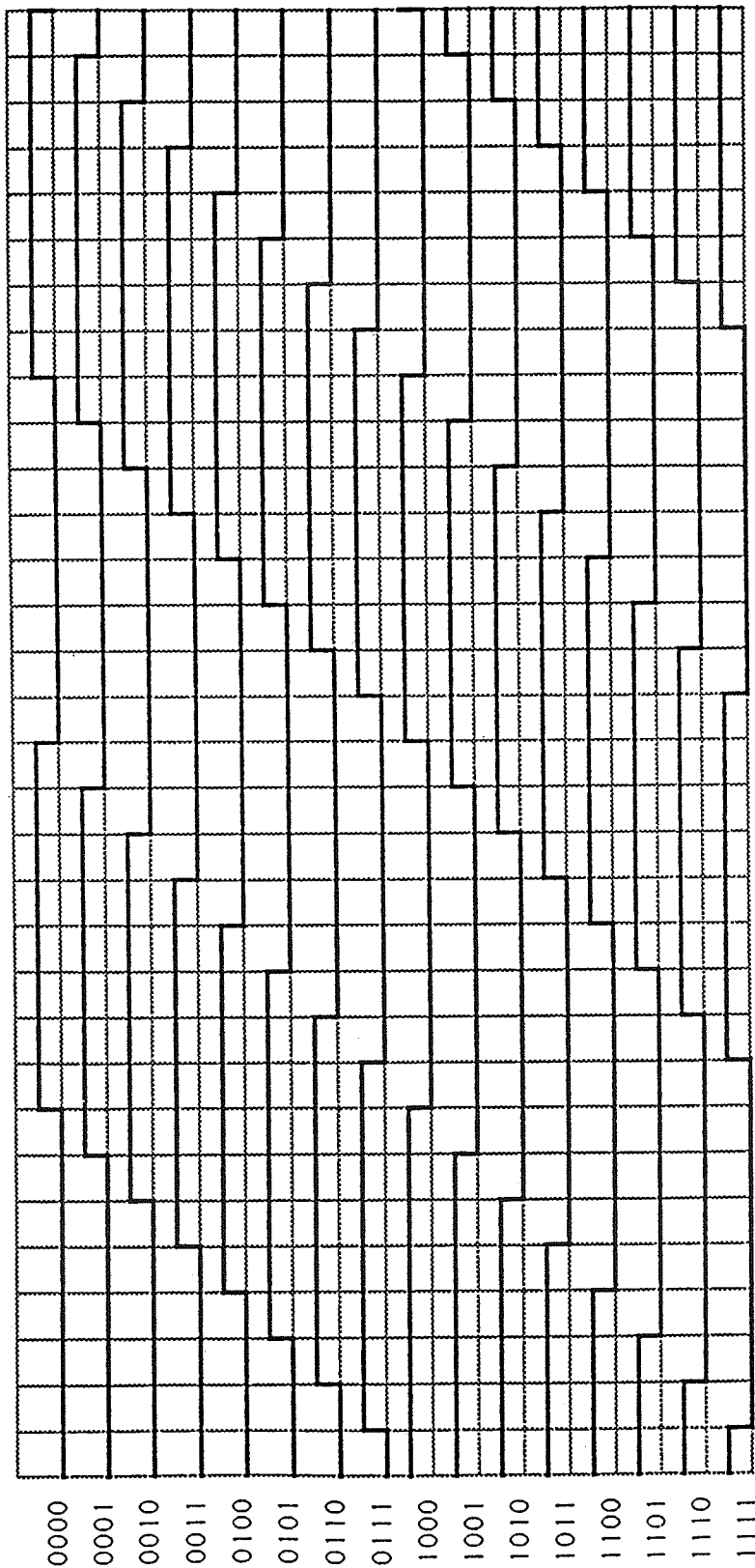


Figure 3.3. Phase Shifted Outputs of a Counter Using Different Presets

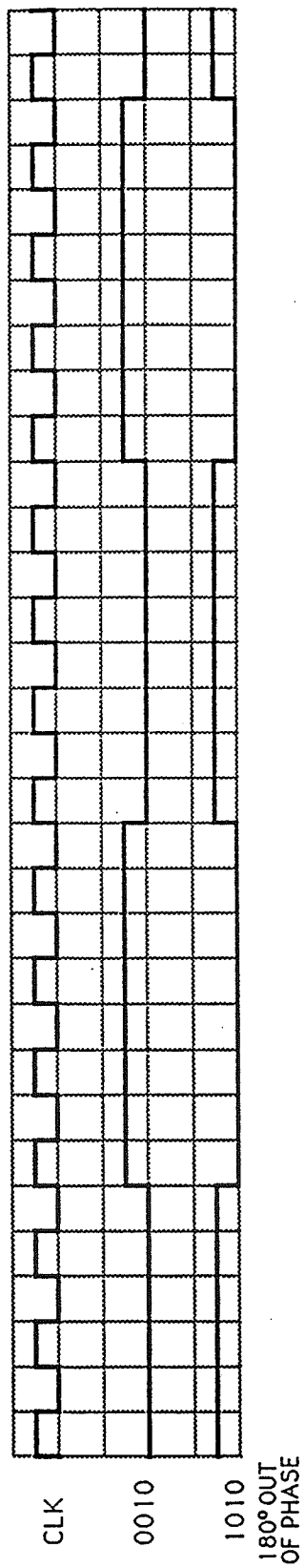


Figure 3.4. Waveforms with a 180° Phase Difference Using the Phase Shifting Technique

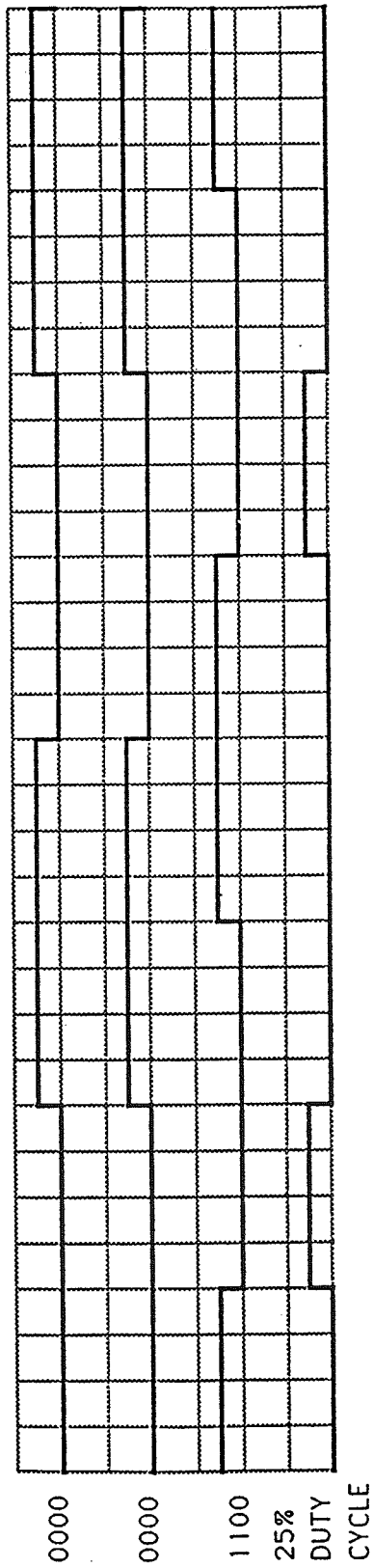
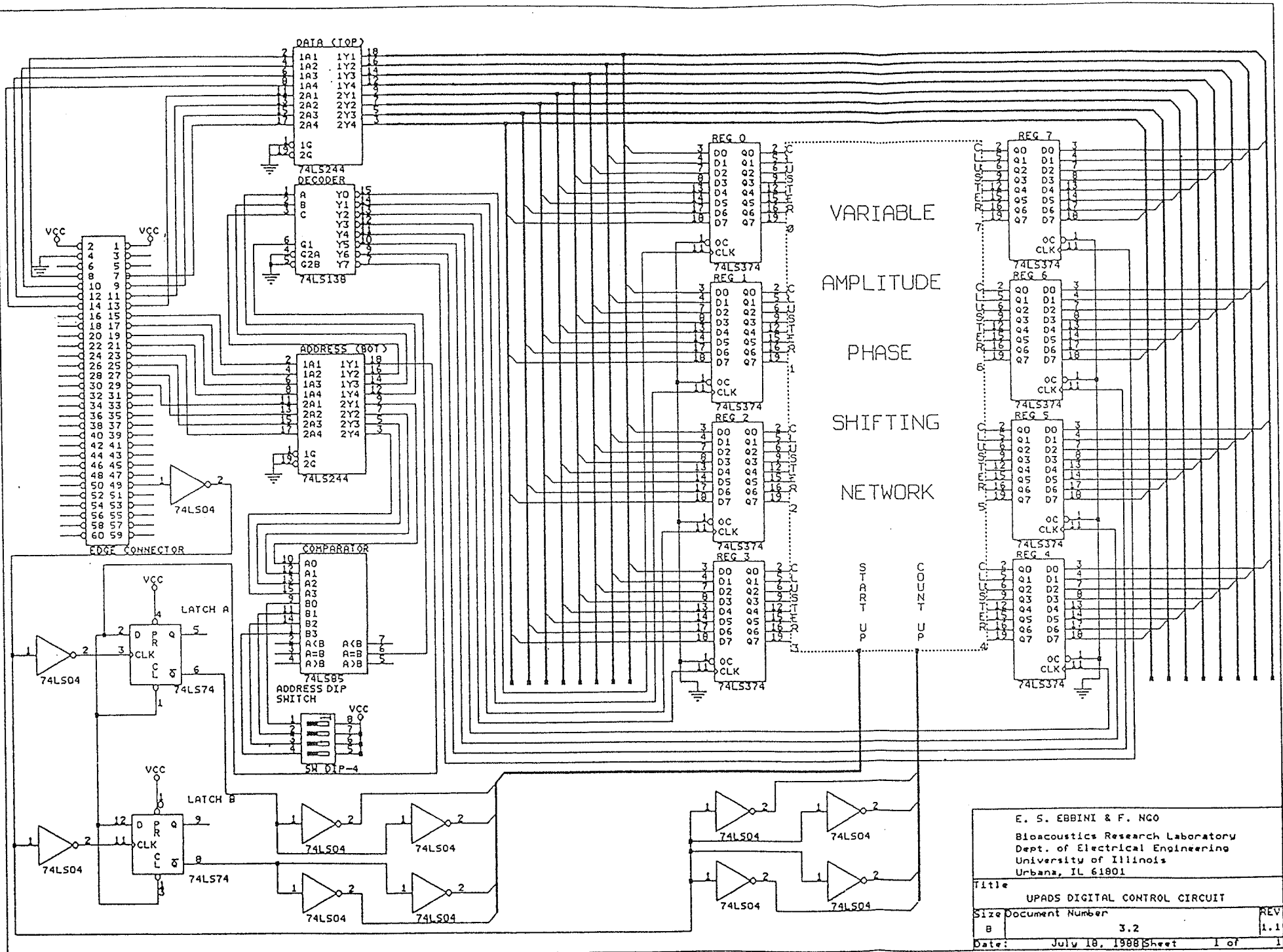


Figure 3.5. Presets Required for a Square Wave with a 25% Duty Cycle and 135° Phase Difference



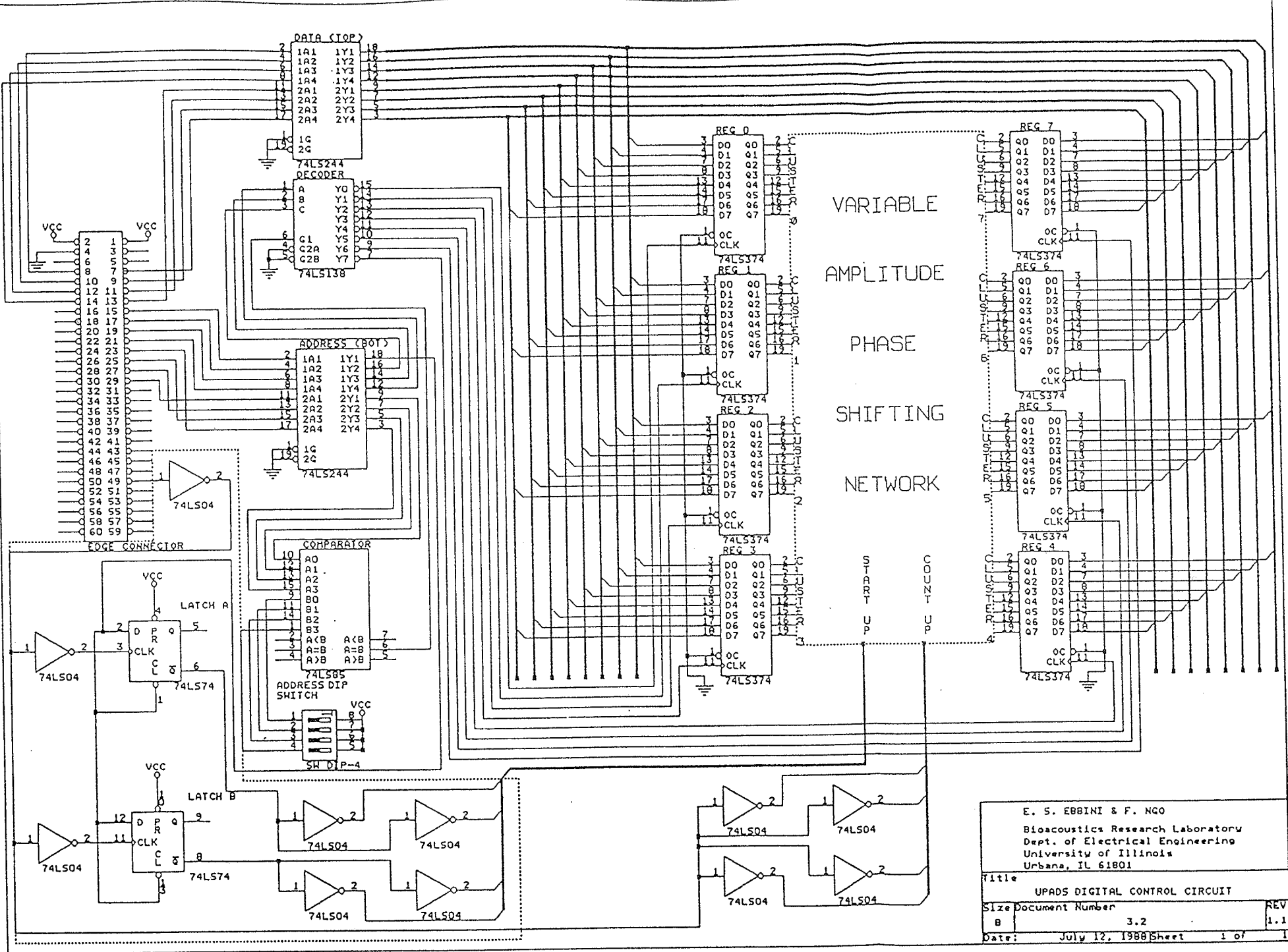
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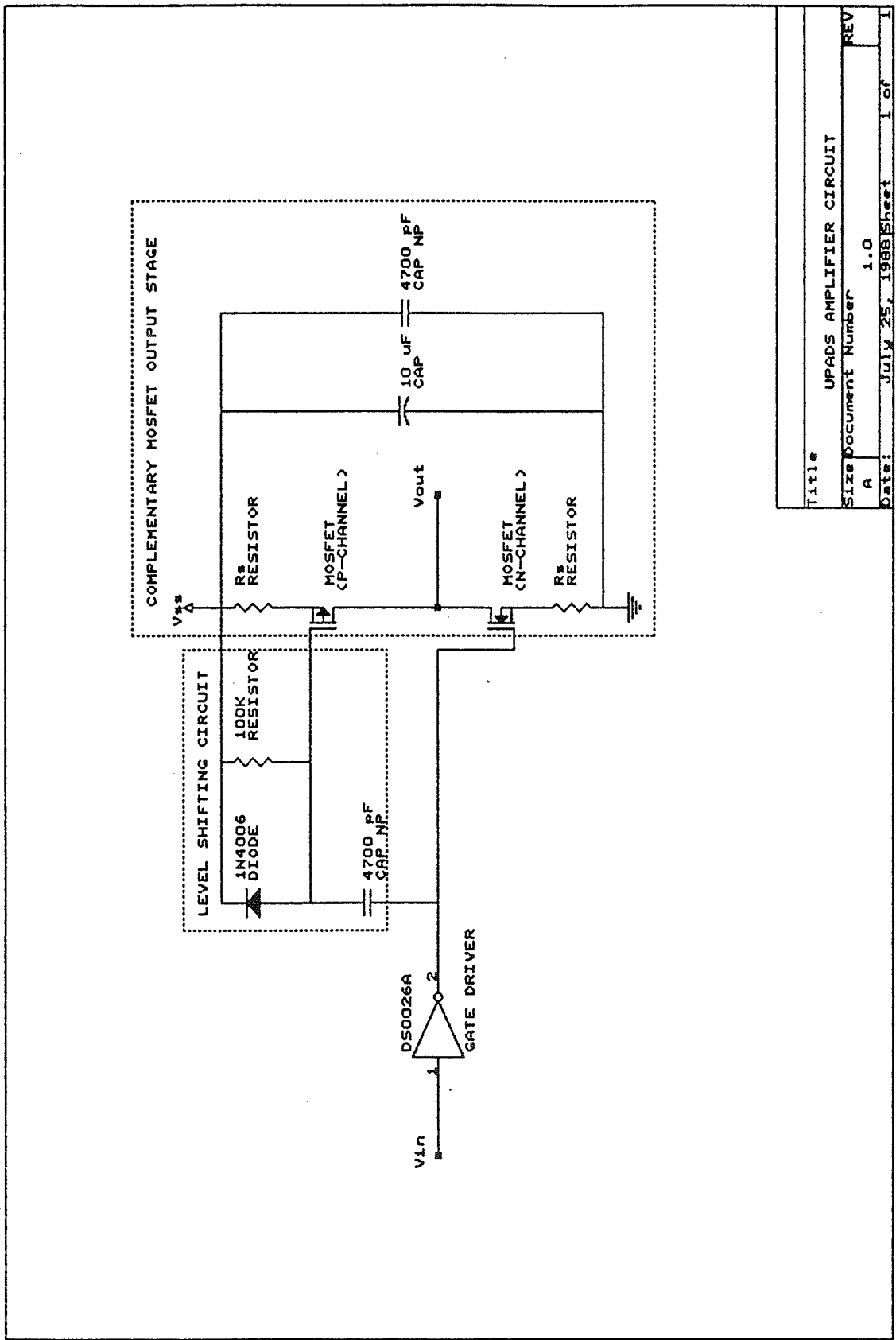
Figure 3.6. The Variable Amplitude Phase Shifting Network Control Circuit



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Figure 3.7. The Load Synchronization Circuit



Title	UPADS AMPLIFIER CIRCUIT		
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Figure 4.1. The Three Components of the Amplifier Circuit

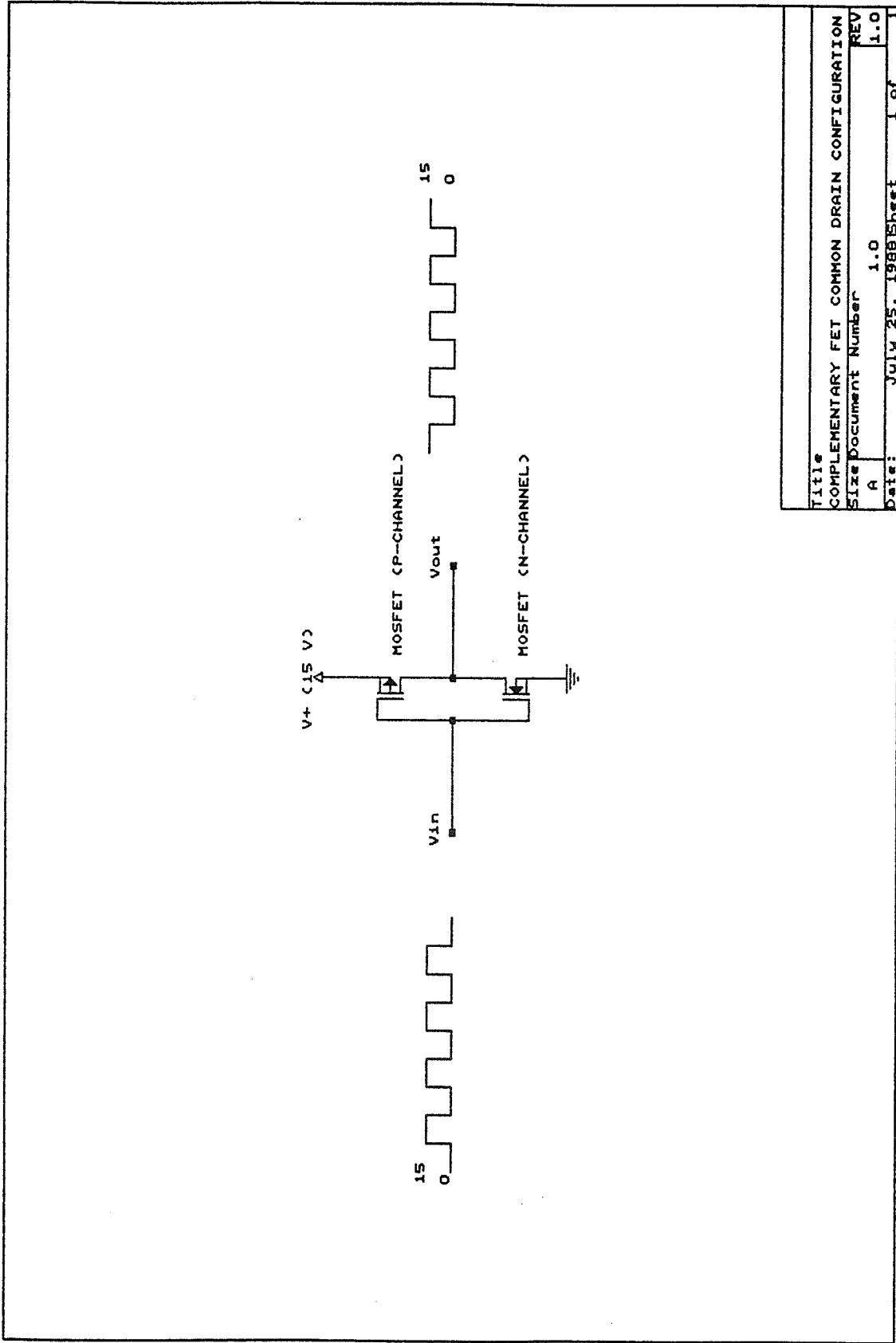


Figure 4.2. The Output Stage of the Amplifier Circuit

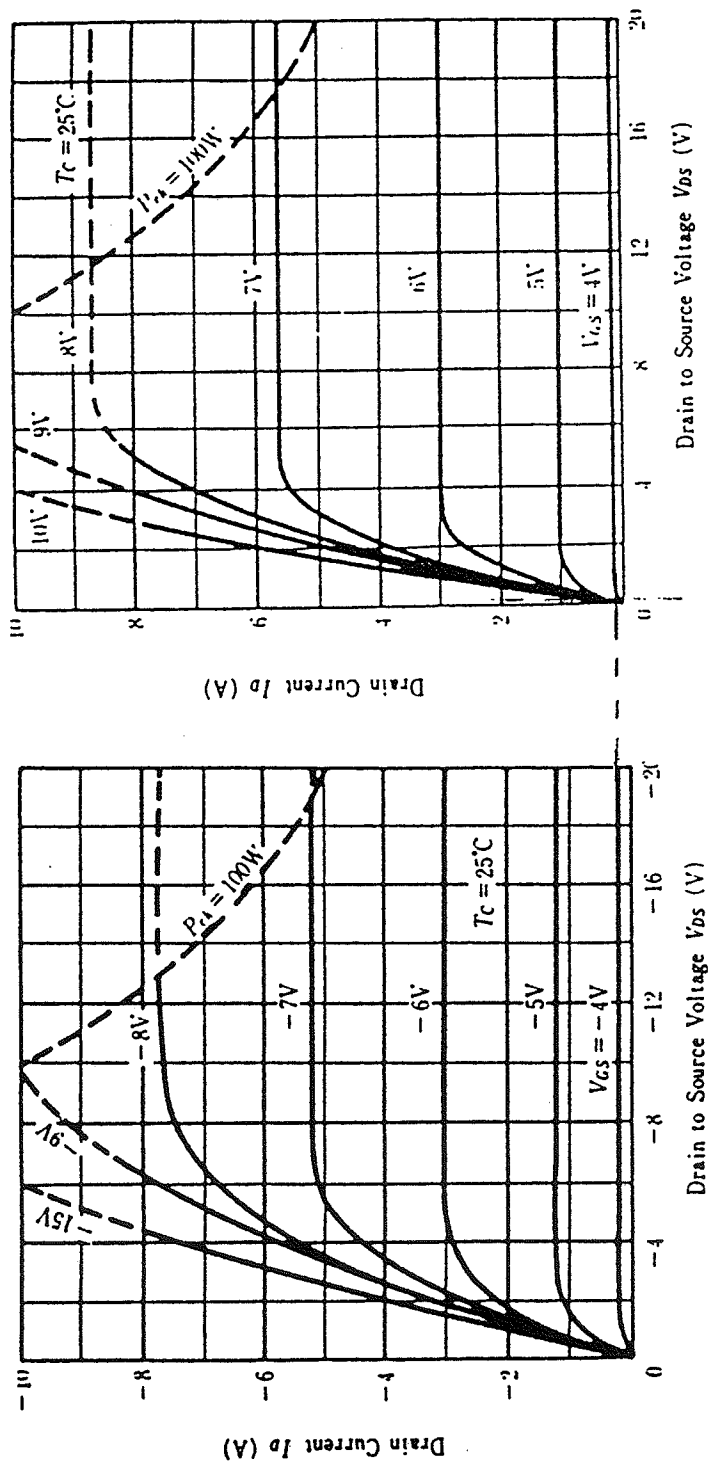


Figure 4.3. Determining the Operating Point of the Amplifier for a High-level Input

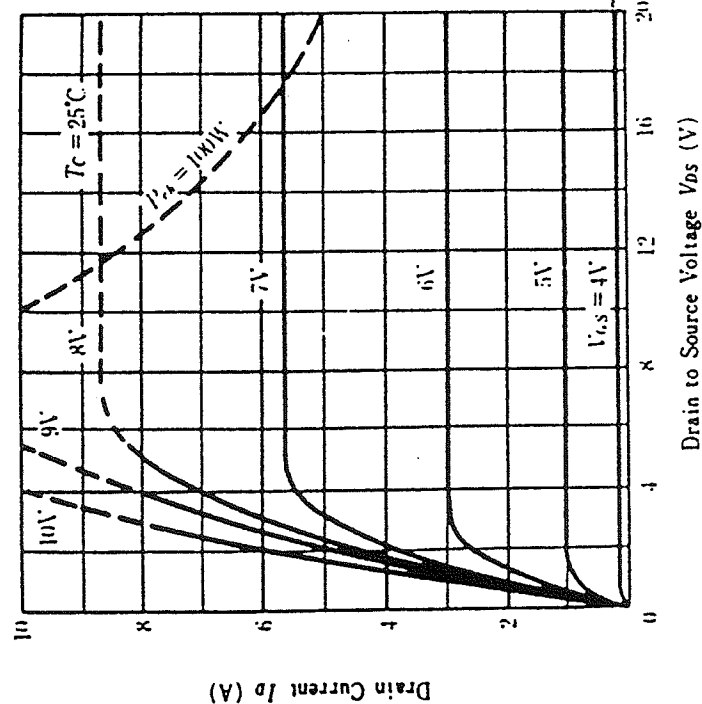
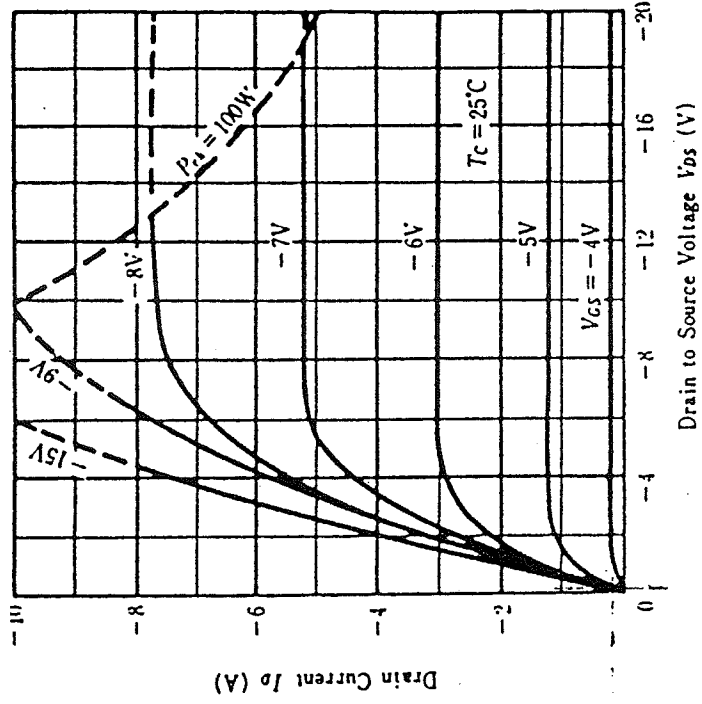
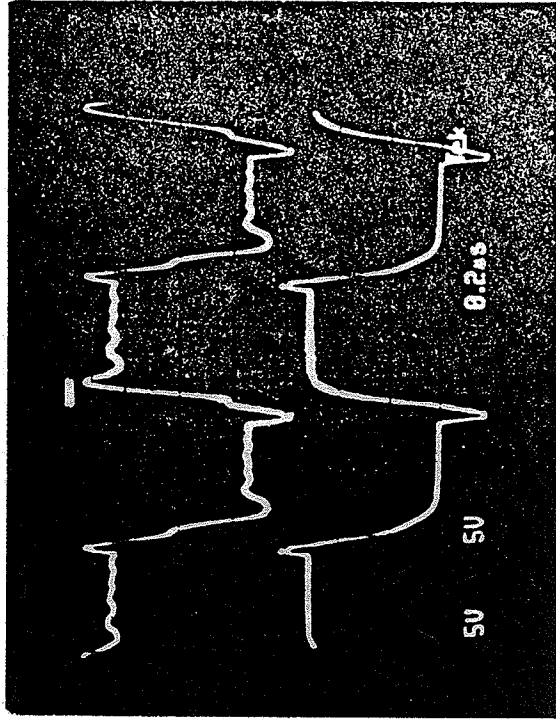


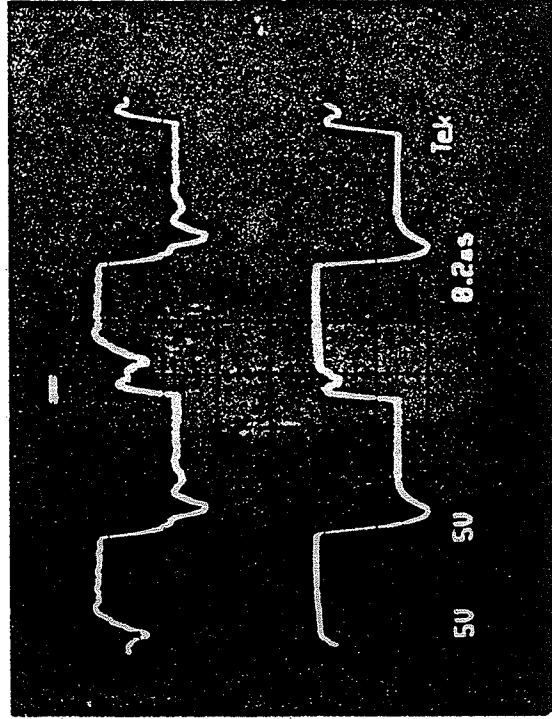
Figure 4.4. Determining the Operating Point of the Amplifier for a Low-level Input



Wire-wound Resistors

Carbon Resistors

Figure 4.5. Effect of Resistor Type on the Output of the Amplifier



Wire-wound Resistors

Carbon Resistors

Figure 4.6. Effect of Resistor Type on the Output of the Gate Driver

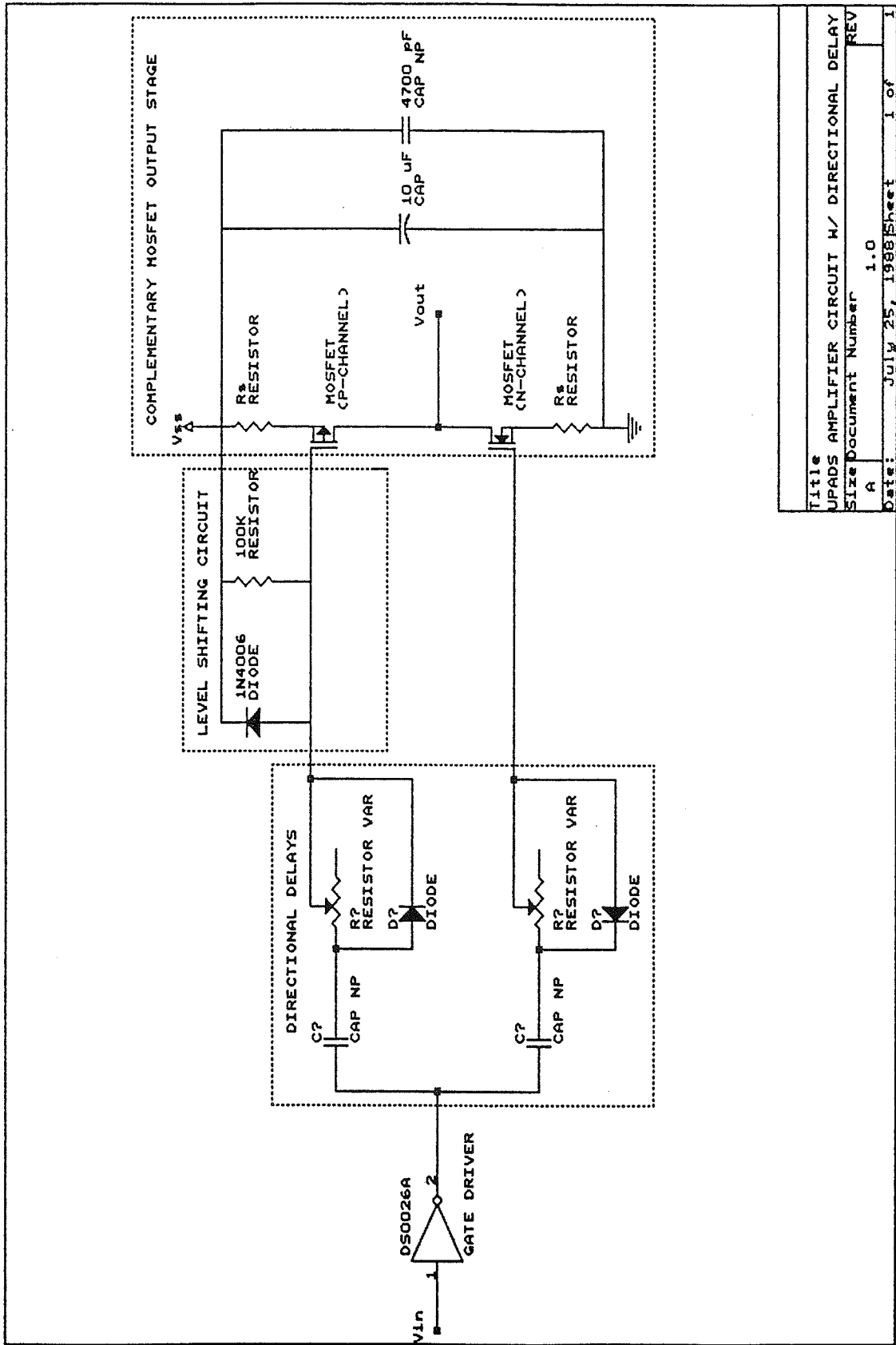


Figure 4.7. Utilizing a Directional Delay in the Amplifier Circuit

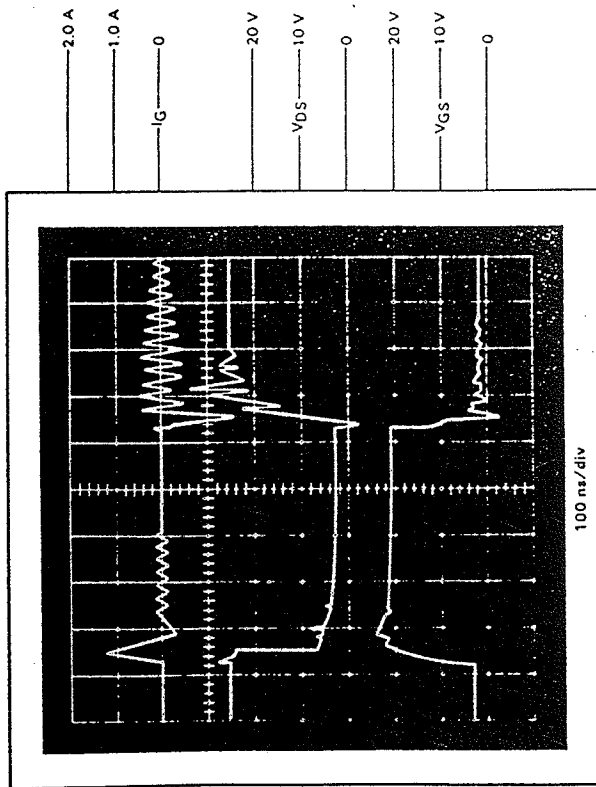


FIGURE 6-27 — POWER MOSFET SWITCHING WAVEFORMS WITH DS0026 CLOCK DRIVER

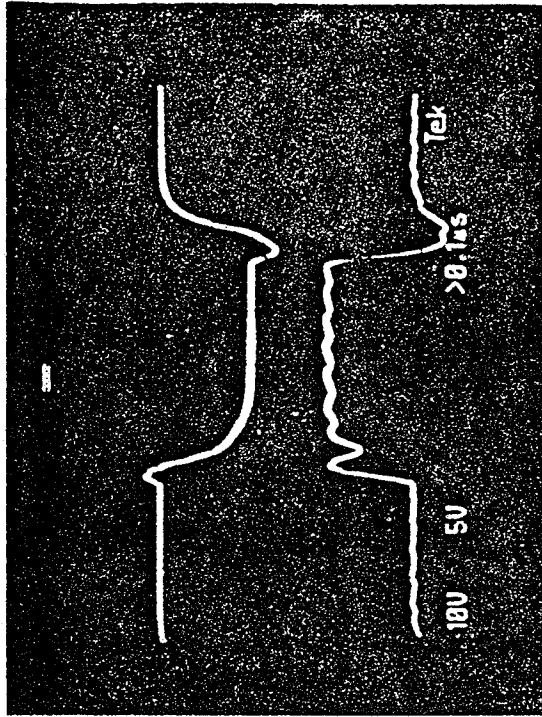


Figure 4.8.a. Output of the Motorola Amplifier

Figure 4.8.b. Output from the UPADS Amplifier

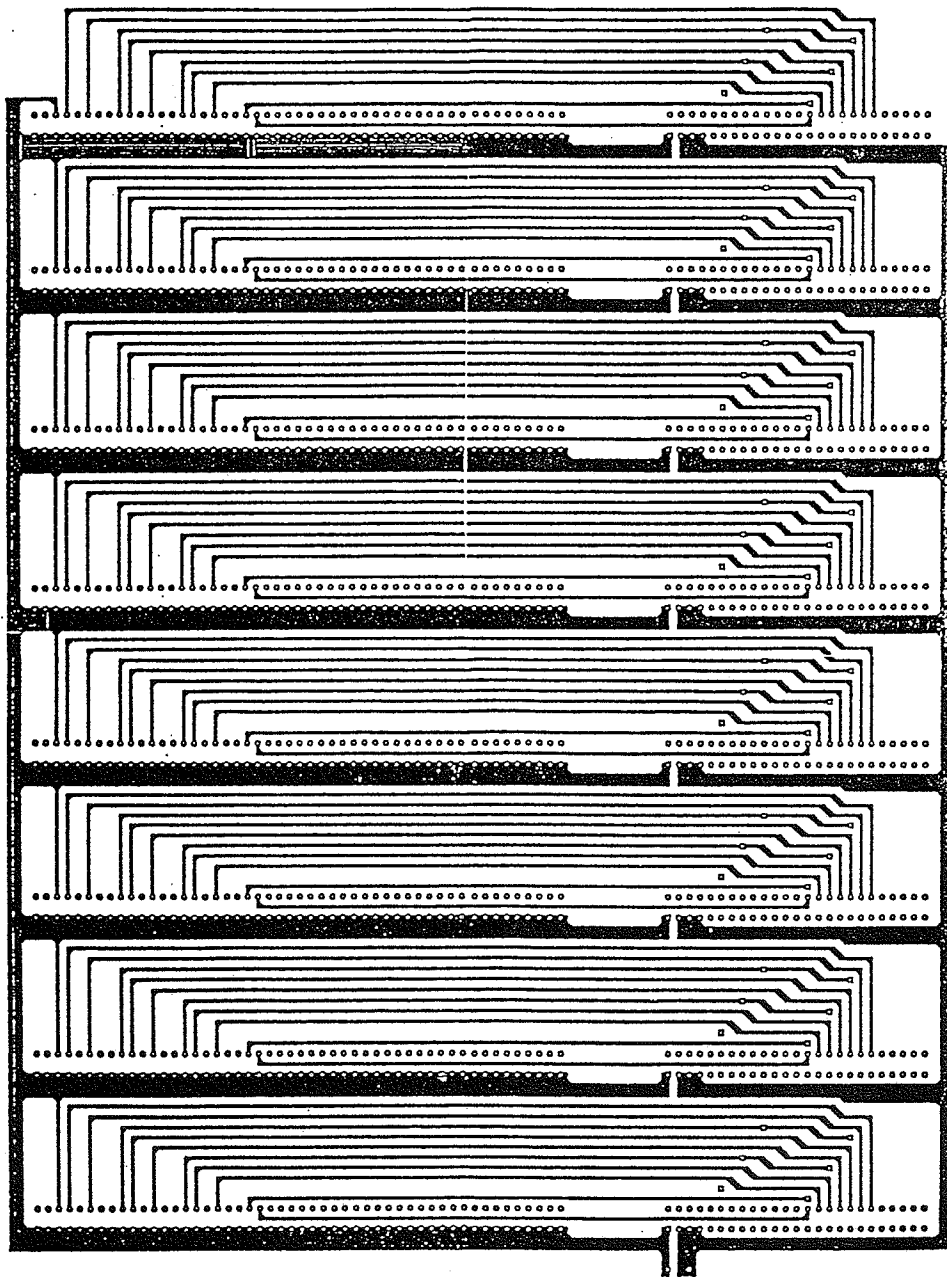


Figure 5.1. Artwork of the High Voltage Bus (Component Side)

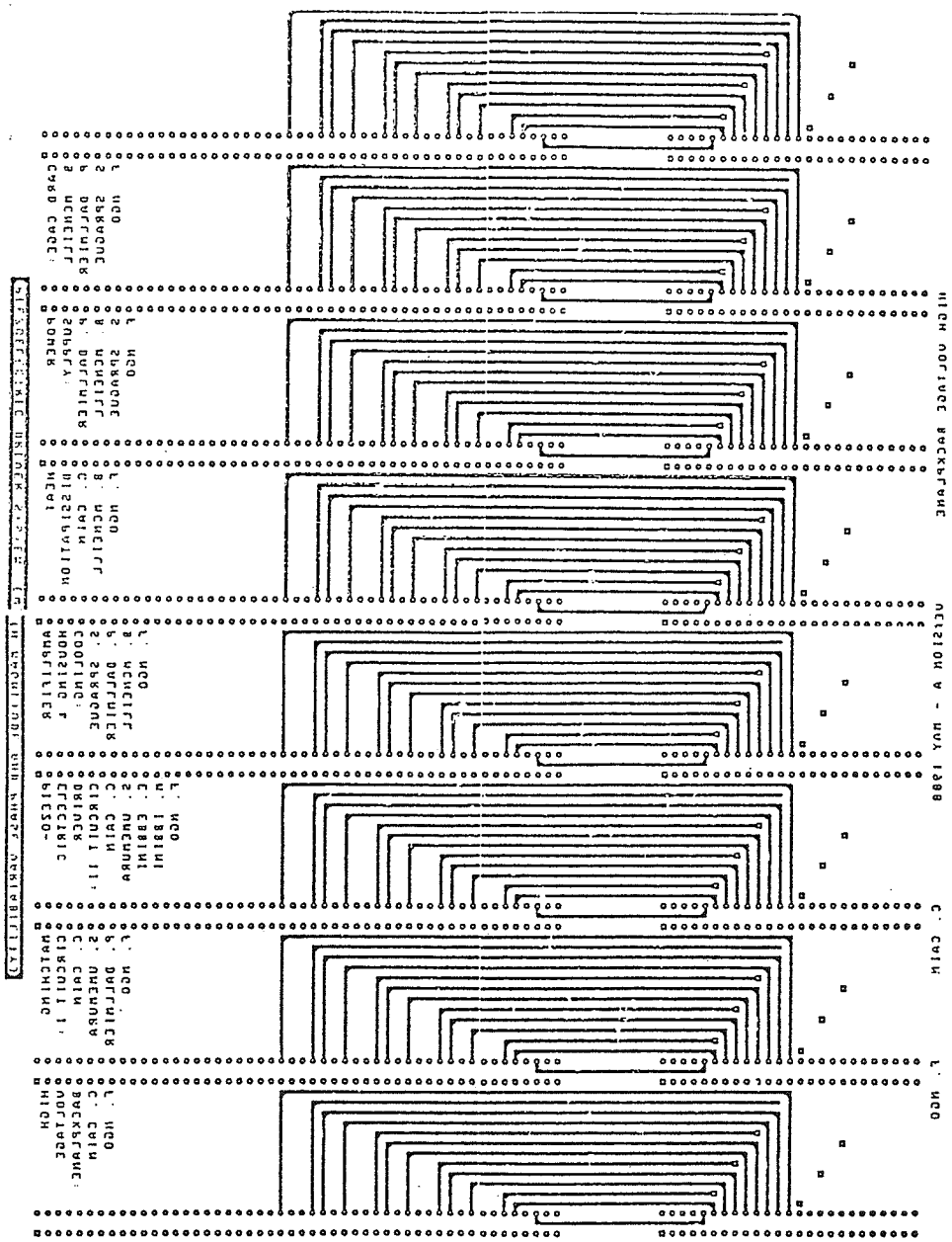


Figure 5.2. Artwork of the High Voltage Bus (Solder Side)

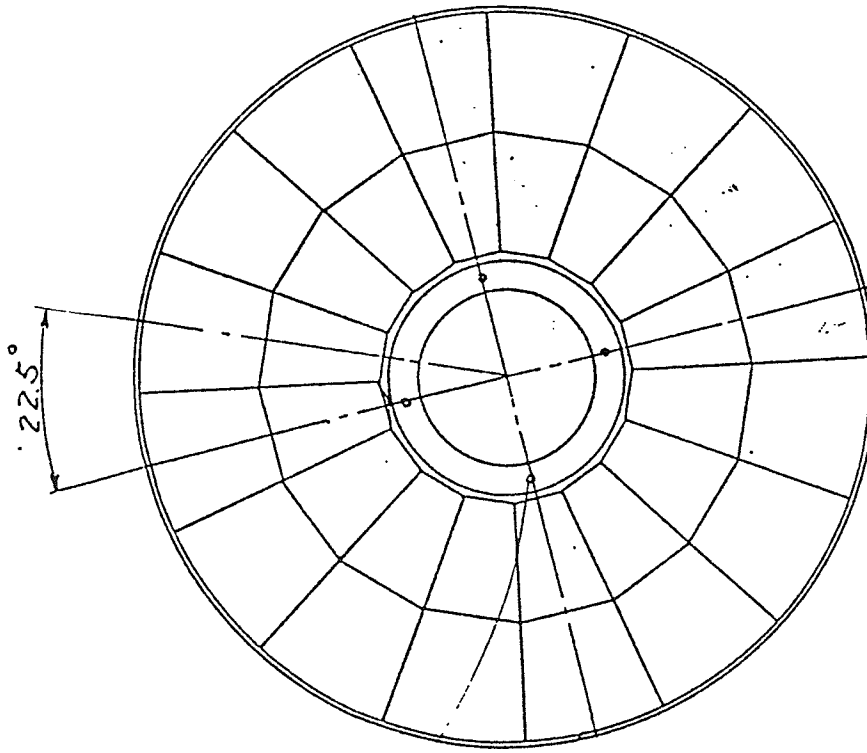
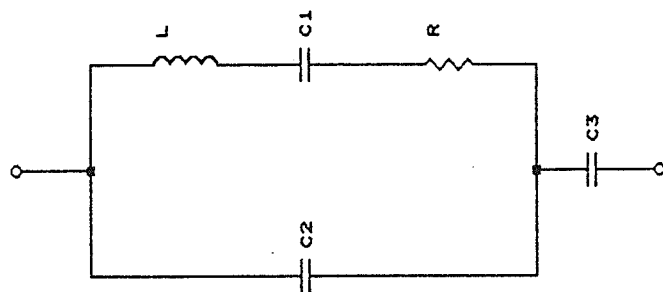
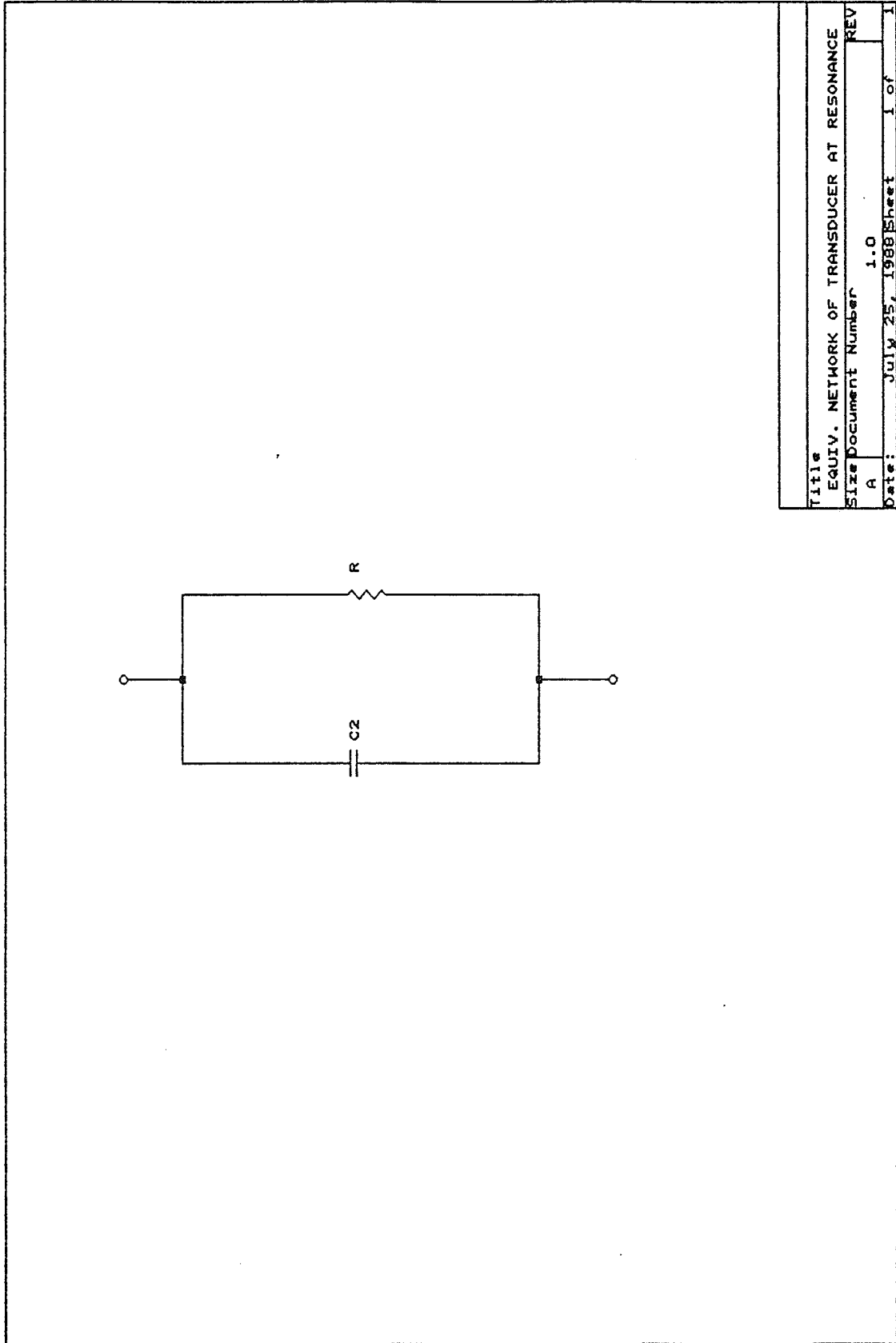


Figure 6.1. Matching Layer for the Sector Vortex Phased-Array



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Figure 7.1. Equivalent Network of a Piezoelectric Transducer



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EQUIV. NETWORK OF TRANSDUCER AT RESONANCE	
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Figure 7.2. Reduced Network of a Piezoelectric Transducer

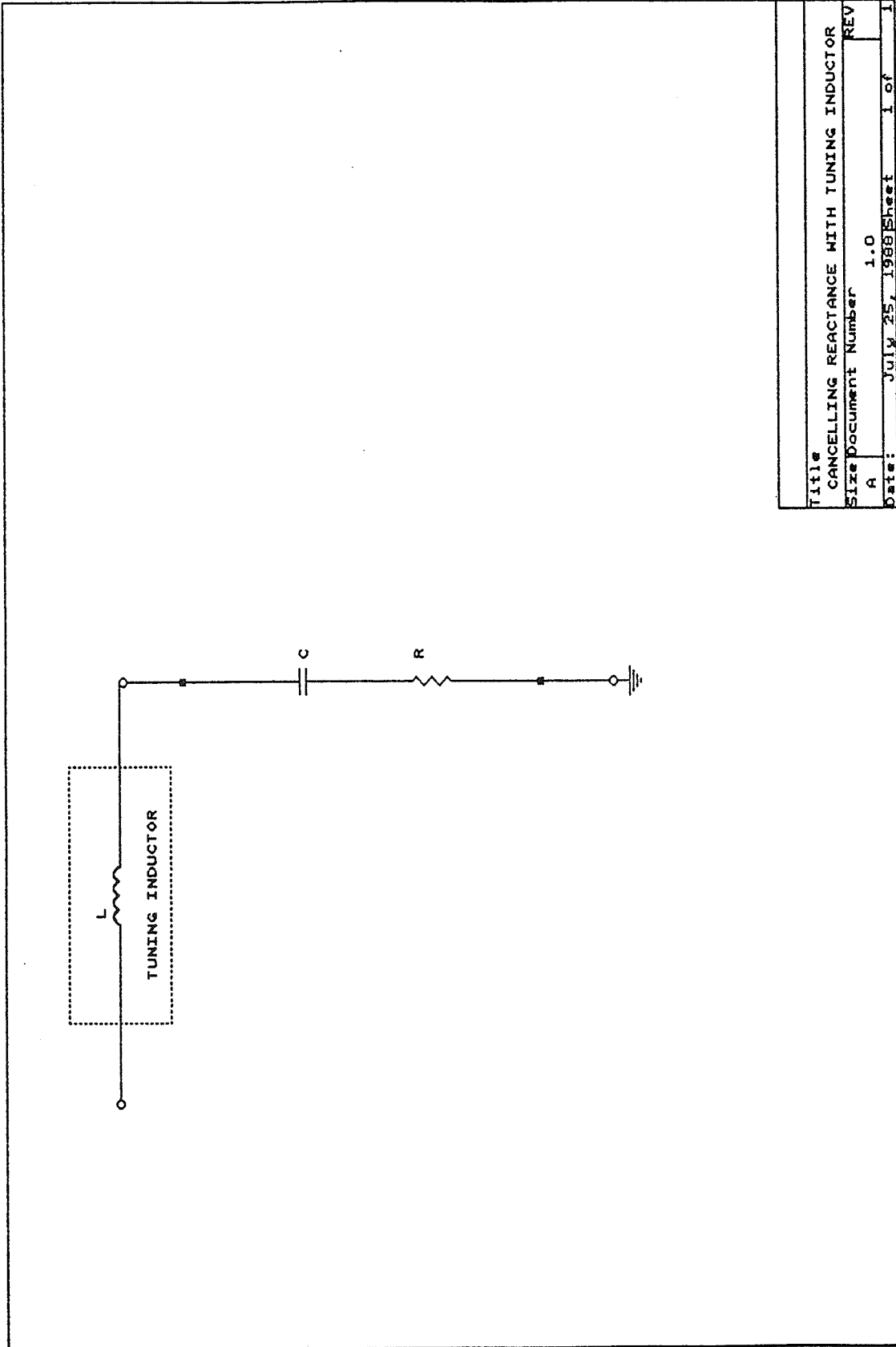


Figure 7.3. Cancelling the Reactance of a Piezoelectric Transducer with a Series Inductor

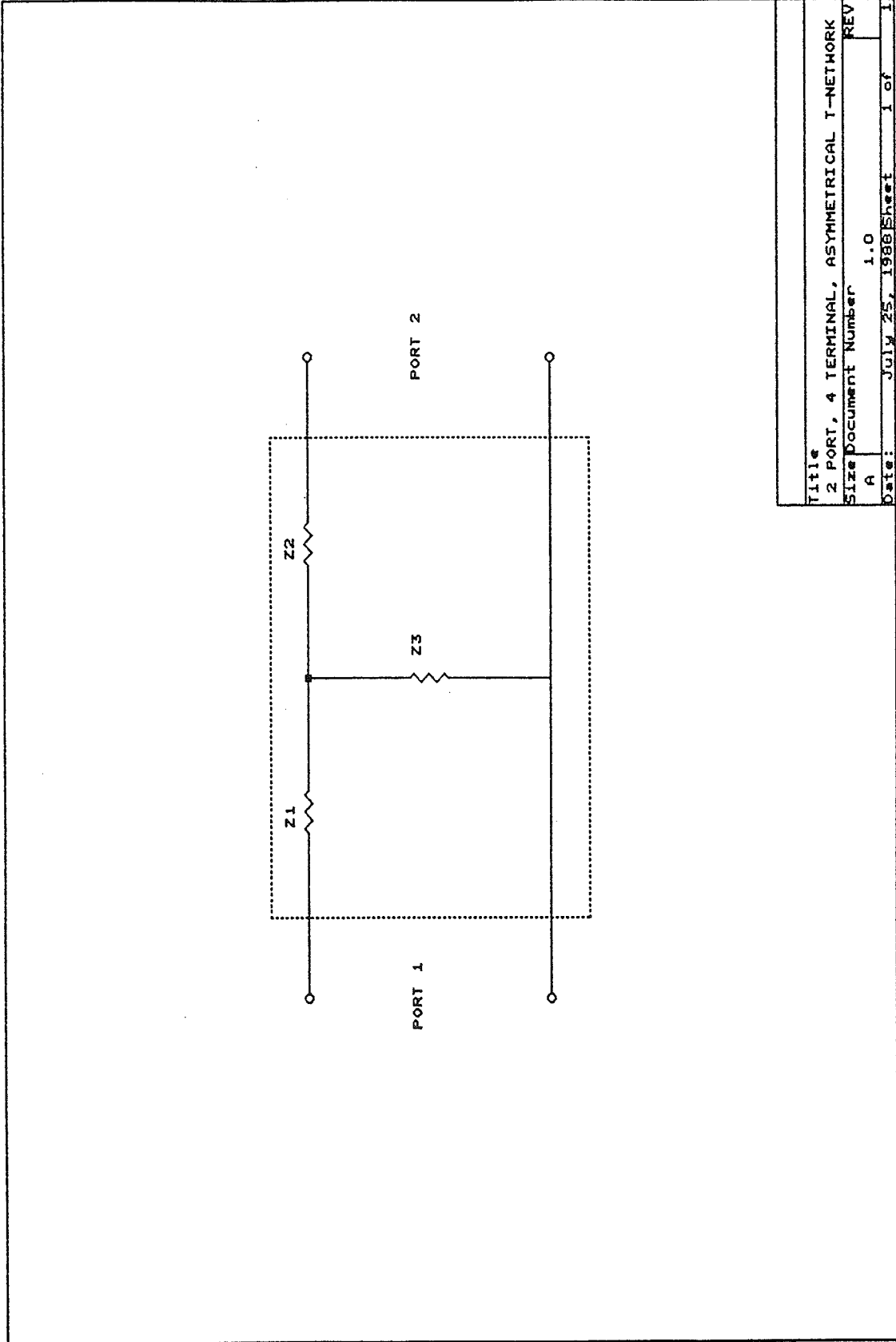


Figure 7.4. The Asymmetrical T-Network Used in the Matching Circuits

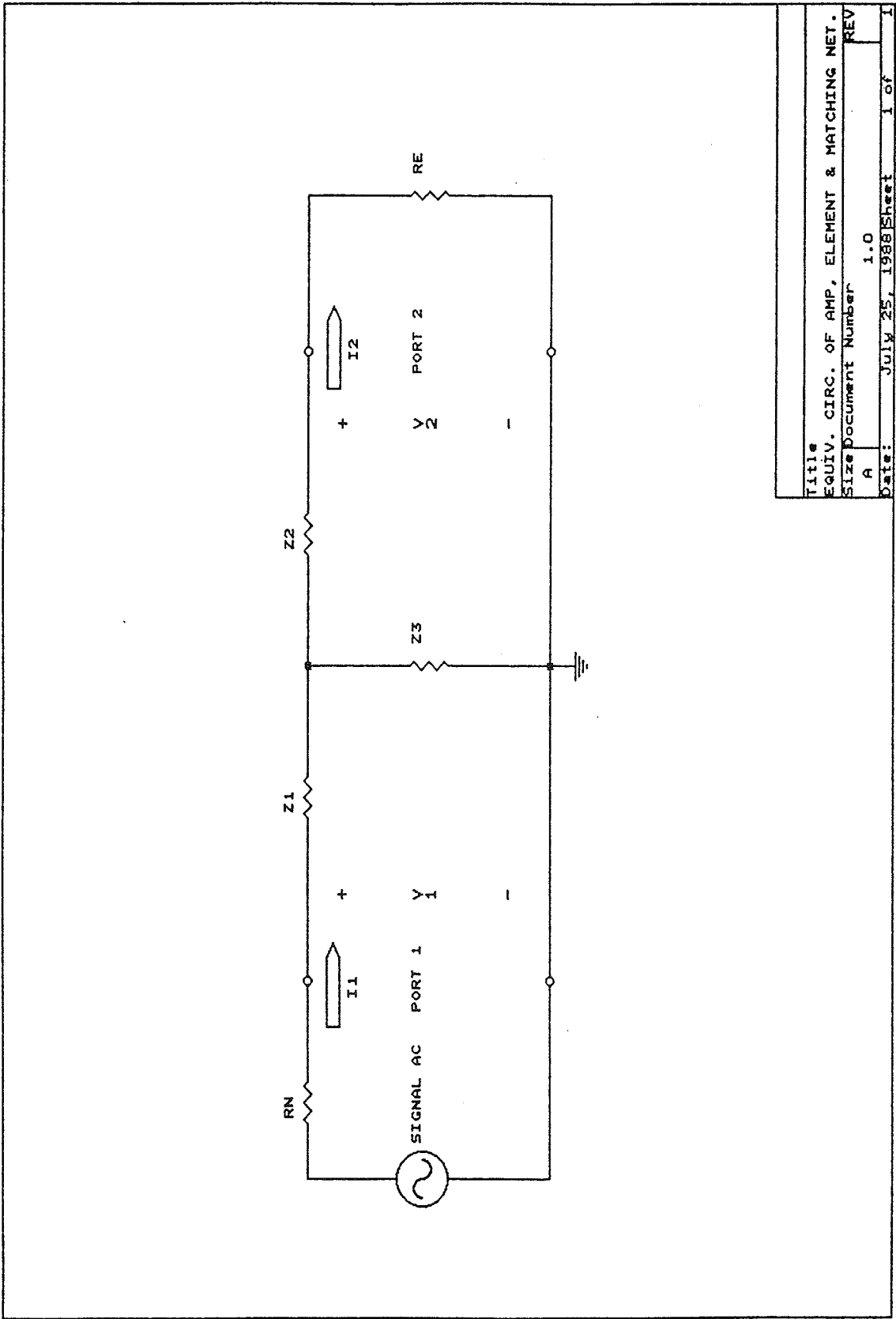


Figure 7.5. Equivalent Circuit of the UPADS Matching System

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