FABRICATION OF A PERFORATED MULTICHANNEL MICROELECTRODE ARRAY

BY

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THESIS

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Above all, I would like to thank my parents, who have foregone their achievements in our homeland to move to this country and make many sacrifices for a chance to better educate their children. They instilled in me self-esteem and taught me that ambition and hard work are the keys to success. Mom and Dad, I thank you for your love and everything you have done for me.

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In graduate school, I gained much more than just knowledge. It broadened my outlook, helped me gain self-confidence, and provided me a with transition to the "real world." I am grateful for the opportunity to pursue a higher education. I shall try my best to contribute to the society that has treated me so kindly.

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CHAPTER 1

INTRODUCTION

Microelectrode arrays provide a new means for neuroscientists who wish to investigate distributed activity in the nervous system. With them scientists can stimulate and record from many neurons at spatial intervals as small as the size of the neurons themselves, as well as to record population field potentials.

An increasing number of researchers have reported the development of microelectrode arrays. Among the different styles of electrodes have been probe-type arrays designed for insertion into brain tissue [Kuperstein and Whittington, 1981; Bement et al. 1986; Pickard, 1979], flexible arrays which conform to the surface of a brain or sense organ [Sonn and Feist, 1974], tubular arrays for nerve fibers [Loeb et al., 1977], regeneration arrays [Edell, 1986] through which severed nerves should regrow, and planar arrays, the topic of this thesis.

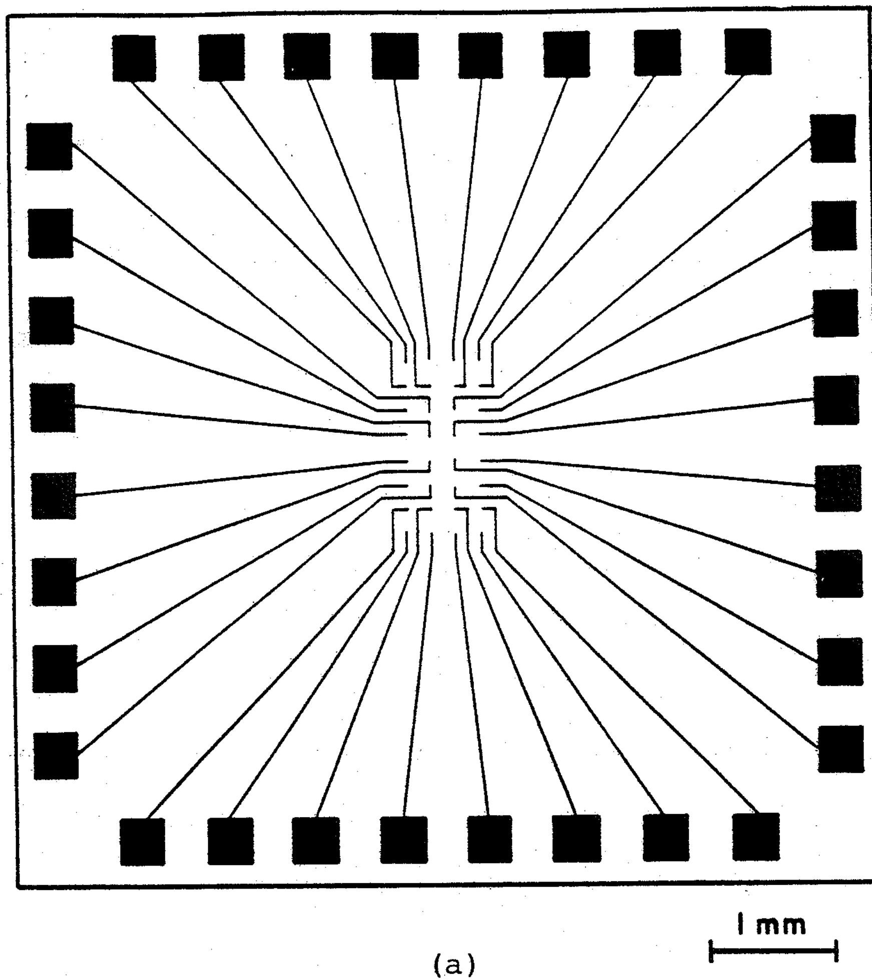
A typical planar electrode array consists of a glass or silicon substrate, photolithographically patterned metal conductors, and an insulation layer (photoresist, polyimide, or silicon dioxide) with holes that define the electrodes. Many processes standard to integrated circuit (IC) technology are used for their fabrication. Most importantly, microelectrode arrays can be fabricated with equipment and materials available to an increasing number of researchers. Planar electrode arrays may possess a large number of channels and can obtain a high volume of data,

which often include two dimensional spatial information about the neural network.

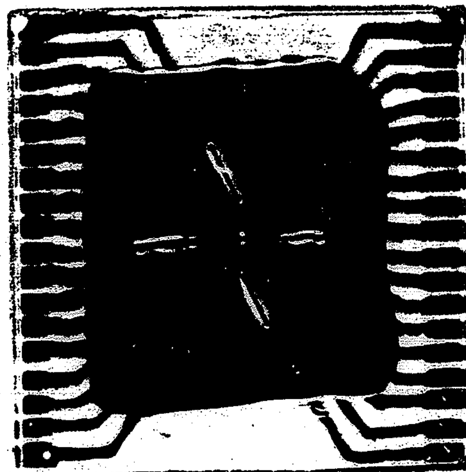
A procedure for producing a planar array has been developed in our laboratory (see Figure 1) [Novak and Wheeler, 1986]. The procedure for positioning all electrodes is simply to place the biological preparation in contact with the array. Since our setup does not use any space on the top surface of the biological preparation, additional conventional electrodes can be placed over the array. In these experiments epileptic signals are recorded from 400 mm thick slices of rat hippocampus, such as those shown in Figure 2.

The duration of these experiments is limited by the health of the preparation. Recording sessions of only 20 minutes have been reported in similar work by Jobling et al. [1981], while Novak and Wheeler [1985] achieved two hours of recording time. In the latter report, conventional electrodes showed that the top half of the slice was active for up to 10 hours. The planar array setup is flawed in that the impermeable array substrate prevents artificial cerebrospinal fluid from contacting the bottom half of the slice. As a result, oxygen diffuses only very poorly from the top surface to the bottom layer of cells in the slice. Hypoxia occurs and the slice dies from the bottom up. Unfortunately, computer simulation indicates that recordable signals are likely to come from only the bottom layers of cells [Wheeler and Novak, 1986].

As a first step aimed at defeating this problem, Ficht [1987] developed a fabrication procedure for a flexible but non-



(a)



(b)

Figure 1. The planar electrode array developed by Novak and Wheeler [1986] shows (a) the central conductor pattern, while (b) a photograph of the finished three inch square array. The electrodes are 25 mm spots at the ends of the conductors in the center of the array.

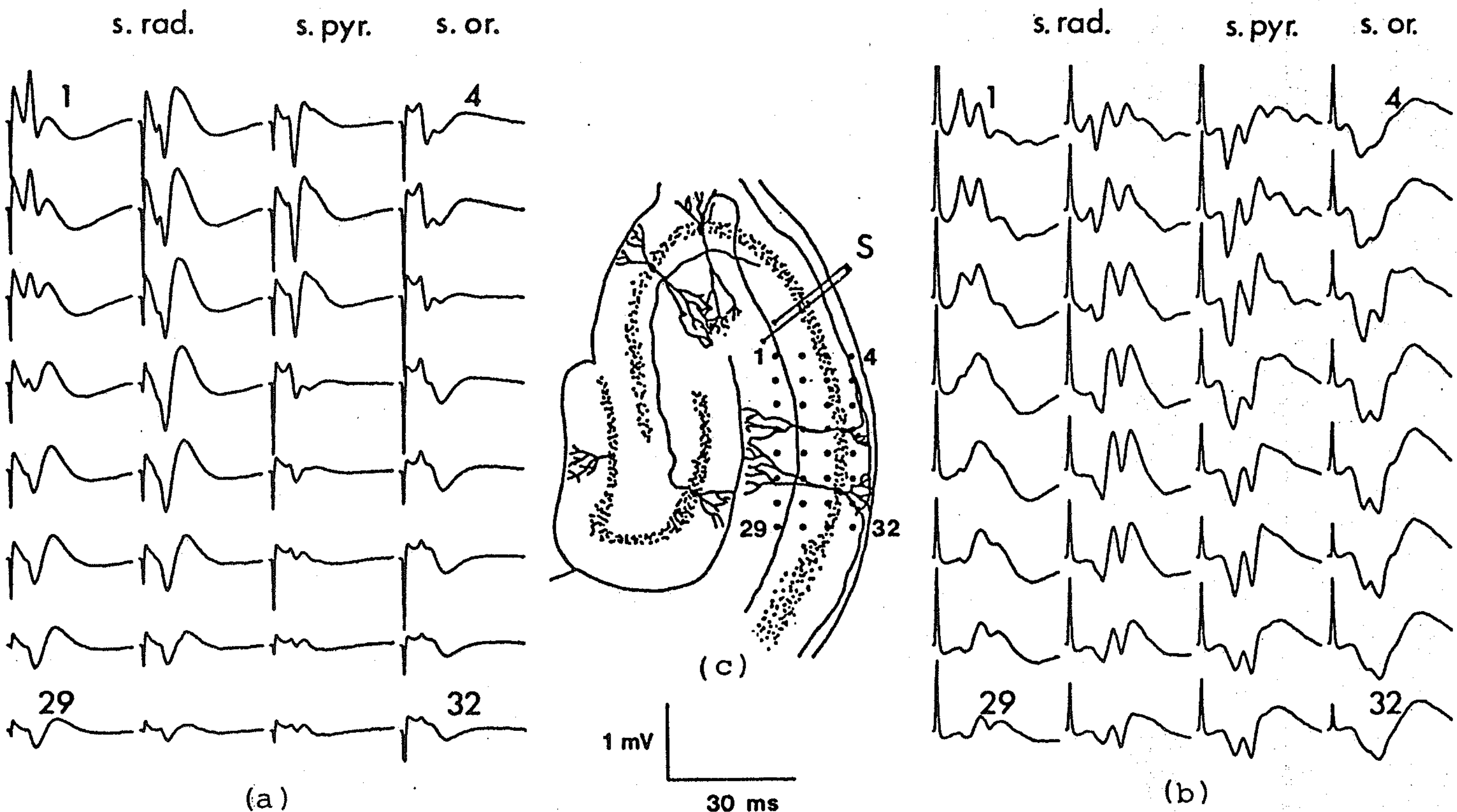


Figure 2. Thirty-two channel evoked potential recordings from a slice of rat hippocampus illustrate the quality of signals obtainable with the array. Those in (a) were obtained in normal media, while the media in (b) included an epileptogenic agent, picrotoxin. The diagram in (c) shows a schematic diagram of the area in the hippocampus from which the recordings were made. [Novak, Ph.D. Thesis, 1988].

perforated array. This thesis reports the continuation of this work to a procedure for fabricating a perforated array which allows a saline solution to come in contact with the slice from both bottom and top. The perforations should increase the supply of oxygen to the slice tissue near the recording electrodes and thus increase the length of the experimental sessions.

The thesis begins with a description of the design issues in Chapter 2. The procedure for fabricating the perforated array is the main result of this work and is described in Chapter 3. Chapter 4 describes some alternate procedures which were investigated and which may be the basis for future modifications of the fabrication schedule. Finally, Chapter 5 summarizes the thesis and suggests applications for the electrode array technology developed here.

CHAPTER 2

DESIGN ISSUES

2.1. Material Used

All material used must be biocompatible, implying both that the materials not be toxic to the tissue and that the typically saline environment not cause failure of the device. Many of the materials used in IC fabrication are biocompatible. Acceptable as substrates and insulators are silicon, silicon dioxide, silicon nitride, and polyimide. Among the relatively biocompatible conductor materials are gold, silver, platinum, indium tin oxide, but not copper.

2.1.1. Silicon substrate

Two inch diameter silicon wafers are chosen to be the substrate, because in general they are very inexpensive, yet provide a flat working surface for many fabrication processes, such as photoresist application and alignment during photolithography. They also provide a rigid surface for wire bonding or other methods of connection to the external devices. The diameter was chosen due to local supply and compatiblity with equipment.

2.1.2. Polyimide

Negatively photosensitive polyimide (Selectilux, E.M. Industries, Hawthorne NY) was chosen because of its ease of use, mechanical stability and strength, and biocompatibility. Several manufacturers make similar products. Non-photosensitive poly-

imide products (such as DuPont Pyralin) require an extra processing step and, as described in Chapter 4, result in poorer control of feature size.

2.1.3. Metal

Gold and titanium were chosen for the conductors. Titanium improves the adhesion at the interface between the gold and polyimide. Gold, the primary conductor, is biocompatible, low in impedance and chemically inert. Although chromium provides better adhesion than titanium, it has been found to form a high resistance alloy with gold during the high temperature (400°C) polyimide cure [Novak, 1985].

2.2. External Connections

The array was designed to take advantage of the hardware in existence in our laboratory, including the amplifiers, connectors, and constant temperature recording platform. The setup was designed for recording from a 3" x 3" glass array. In this setup, a water bath maintains a constant temperature (typically 34°C) in a chamber in physical contact with the bottom of the array. Custom edge connectors lead to two banks of 16 channel amplifiers. An adapter is needed to connect the new array to the existing edge connectors.

2.3. Mask Design Considerations

Three masks were needed, including a perforation mask, a conductor mask, and an insulation mask. The new array duplicated the

geometry of an array in use in our laboratory, i.e., 32 channel in a 4 x 8 arrangement, with 200 mm separations between electrodes. A line width of 25 mm was chosen to eliminate the possibility of lift-off of the pattern due to undercutting during the etching procedure. This was not a fundamental restriction on the geometry. The old geometry is reproduced for compatibility with previous results.

Requirements for the new masks follow.

2.3.1. Perforation mask

The perforation mask was used to pattern the base layer polyimide. The perforations were designed so as not to overlap with the conductor path. To promote saline flow, the perforation area should be maximized. However, to preserve the integrity of the polyimide film and the continuity of the conductor path, the perforations should be limited. Since this limit was not known, a conservative design was made. As experience is gained, it may be appropriate to use a design in which the array looks more like a net with conductors along the threads than like a film with holes in it.

The alignment marks included eight evenly spaced dots on a two inch diameter circle that circumscribes the wafer. The dots were used to position the perforation holes in the center where the wafer is etched through. Several gross alignment marks and fine alignment marks were used to aid rapid alignment of the wafer. Since the light sensitivity of the polyimide material is negative, a light field mask is required. The perforations were

chosen to be 20 mm squares and 20 x 100 mm slits. The perforation mask is shown in Figure 3.

2.3.2. Conductor mask

The conducting leads were chosen to be rectangular with a 25 mm width. Since ribbon cables were chosen for external connection, the bonding pads were designed to match the dimensions of ribbon cables. Thus, the center-to-center distance is one twentieth of an inch, and the pad width is one fortieth of an inch. The center of the device provides sufficient area for maneuvering the slice during recording.

The conductor mask is shown in Figure 4, along with an enlarged view of the central region with both the conductors and perforations.

2.3.3. The insulation mask

This mask includes the perforation hole pattern plus the electrode hole pattern. Thus, the mask (Figure 5) includes the pattern of Figure 2, the matrix of 4 x 8 squares for deinsulating the tips of the electrodes, and various alignment marks.

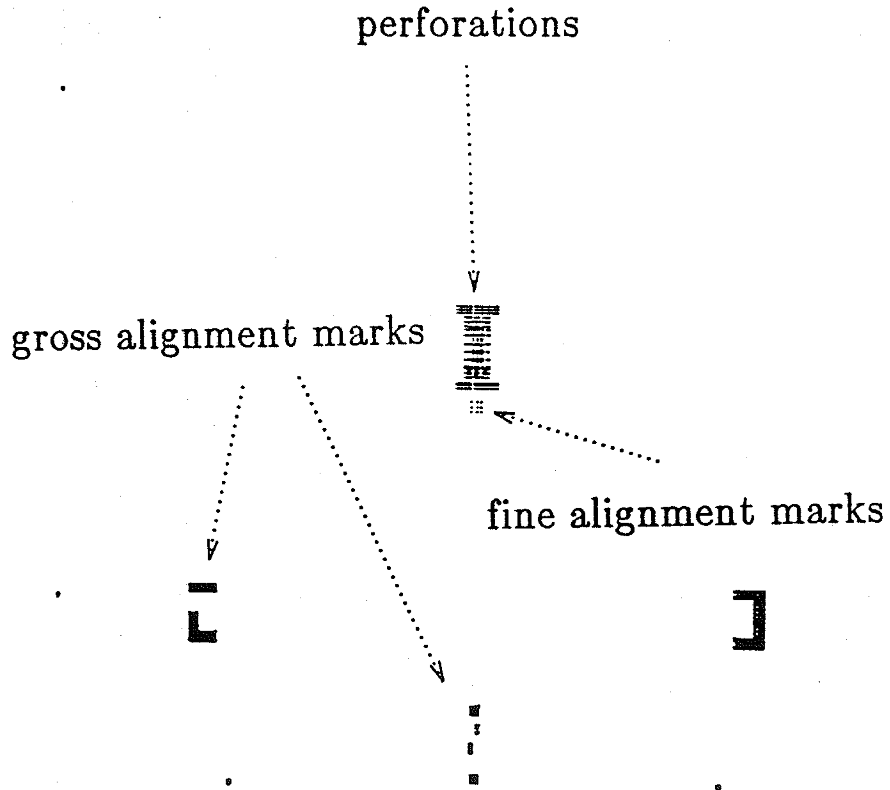


Figure 3. The perforation mask.

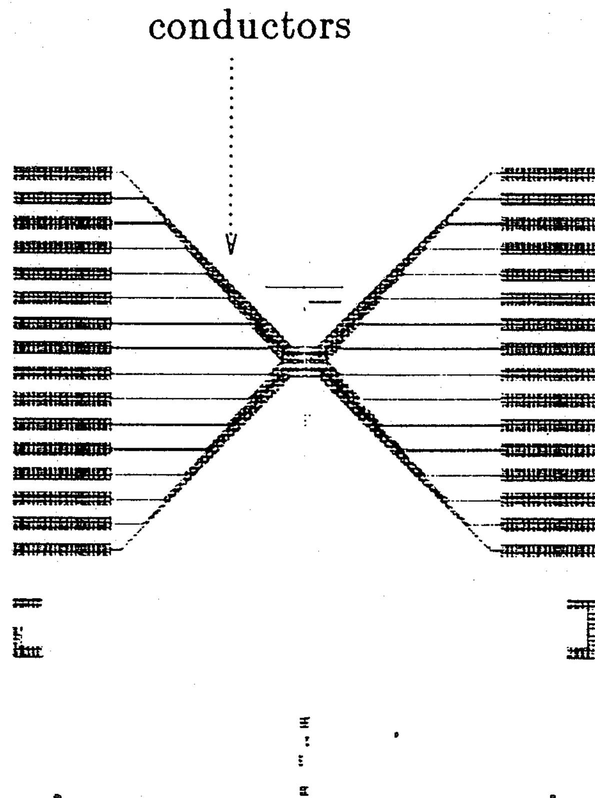


Figure 4(a). The conductor mask.

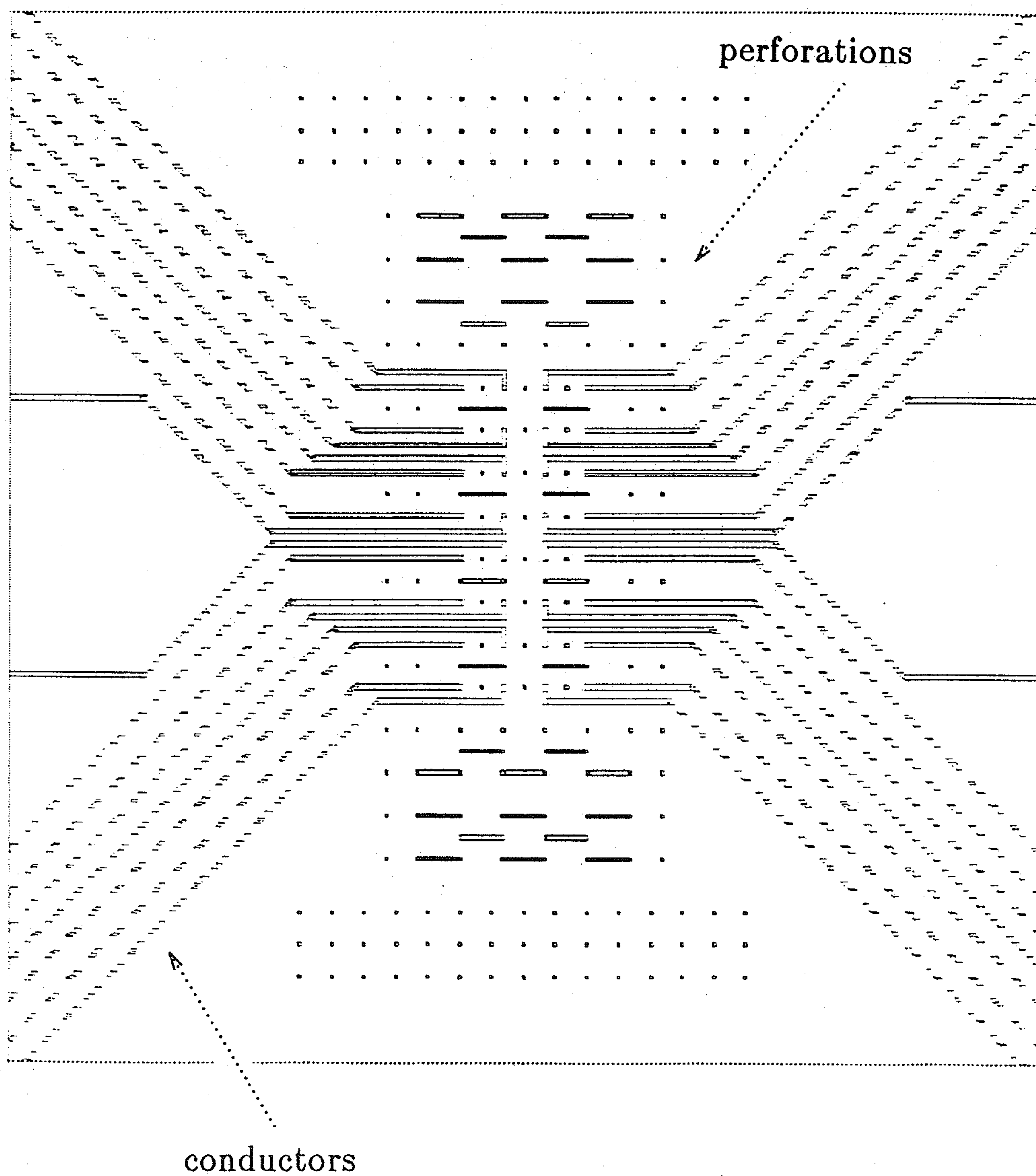


Figure 4(b). The central region of the conductor and perforation mask.

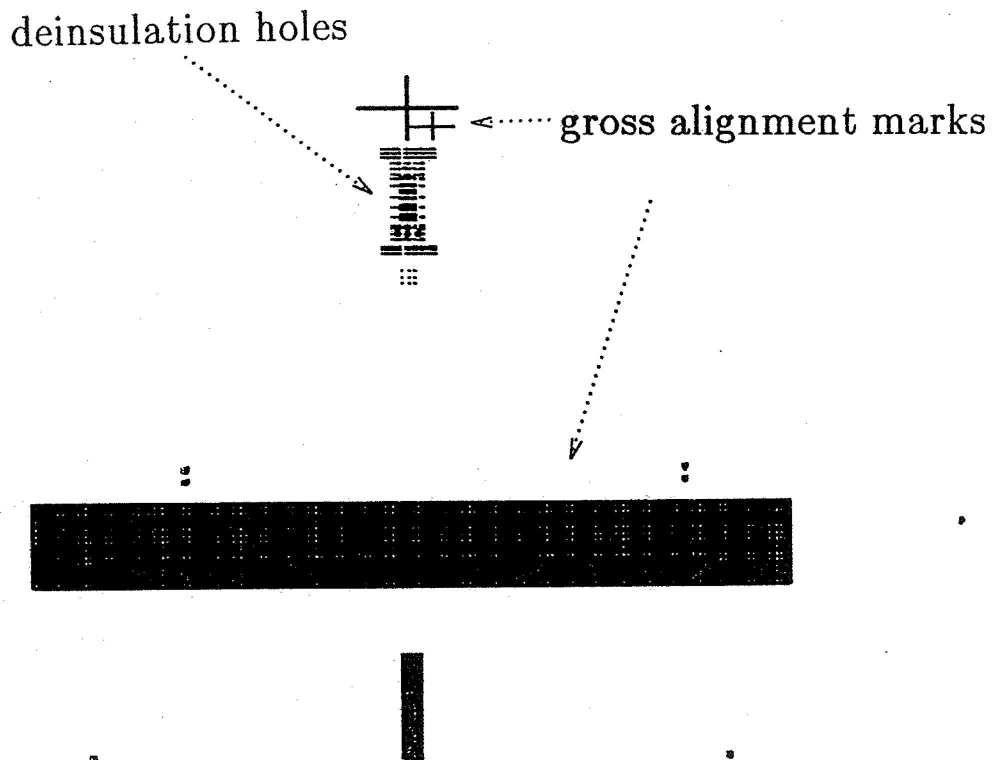


Figure 5. The insulation mask.

CHAPTER 3

FABRICATION PROCEDURE

3.1. Overview

The objective of the fabrication procedure is to construct the array on a free standing, perforated, polyimide diaphragm on a two inch diameter silicon wafer, which has been processed to look like a washer.

After the array structure is patterned on the front side of the wafer, a hole is etched from the backside through to the bottom polyimide film of array. A 7 mm by 7 mm window etched into the backside silicon dioxide acts as a mask for the anisotropic etching of a square cavity 70 - 80% of the distance through the wafer from the backside. This technique maintains a sharply defined geometry through the wafer. Next, the base layer of polyimide film is constructed. The remaining fabrication procedure includes metalization, insulation, and electroplating. Finally, isotropic etching of the wafer from the back side completes the removal of the silicon from the polyimide diaphragm.

3.2 Wafer Prethinning

Wet oxidation is carried out to grow silicon dioxide (approximately 1.2 mm thick) to serve as the masking material for this step. Photoresist (PR, Shipley AZ 1450J) and photolithographic techniques are used to define the geometry of the oxide window where the wafer will eventually be etched through. The alignment is done using the profile, including the principal flat, of the

wafer as reference (Figure 6). The mask for this step was hand-made.

Buffered hydrofluoric acid (6:1 NH_3F:HF) is used to open the oxide window. Photoresist is used to protect the front side of the wafer during this step. When this step is finished, the PR is removed with acetone. The wafer is then immersed in an anisotropic etchant (hot potassium hydroxide (KOH), or ethylene diamine pyrocatechol (EDP)) [Bassous and Baram, 1978] to yield the desired cavity. The wafer is cleaned by soaking in warm water for 10 minutes followed by deionized (DI) water rinse, and dried with blown nitrogen and a high temperature (100°C) bake.

These procedures are outlined in Table 3.1.

Table 3.1

Wafer Prethinning

1. Oxidize the wafer (see Appendix).
2. Frontside protection
   a. spin PR on the shiny side of the wafer at 3000 rpm for 30 seconds.
   b. bake at 90°C for 20 minutes.
3. Backside PR patterning
   a. spin PR on the backside of the wafer, 3500 rpm, 30 seconds.
   b. bake at 90°C for 20 minutes.
   c. use the oxide mask to expose the backside for 45 seconds.
   d. develop the PR in PR developer (1:1 DI:Shipley Microposit Developer).
   e. hardbake the wafer at 130°C for 20 minutes.
4. Create the oxide window by floating the wafer, PR window side down, on buffered HF (6:1 NH_4F:HF) for 5 minutes to open the oxide window.
5. Etch the wafer in 105°C EDP solution for two and a half hours (3 g pyrocatechol, 8 ml H_2O, and 17 ml ethylene diamine).
6. Remove and soak the wafer in warm DI for 10 minutes.
7. Rinse and blow dry.

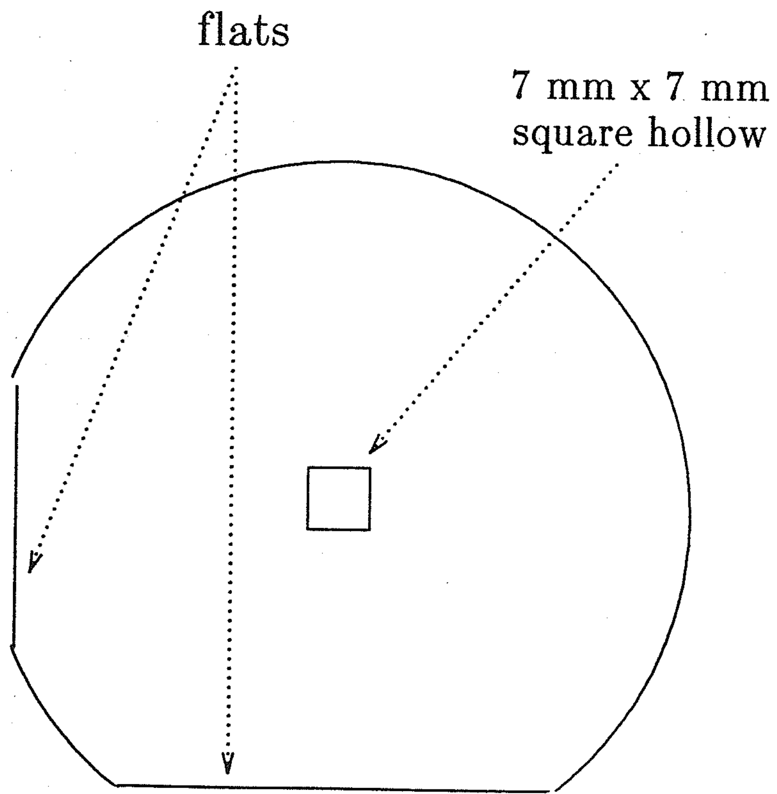


Figure 6. The backside etching mask.

3.3 Polyimide Coating

Selectilux HTR-100 polyimide [EM Industries, Hawthorne, NY] is applied to the center of the wafer, which is spun to yield a layer with uniform thickness. The polyimide is softbaked and photopatterned with the perforation mask and a mask aligner (a Kasper aligner in the ECE Department clean room facility). Finally, it is postbaked then fully cured. The thickness of the film is approximately 2 - 3 mms. This is the base layer of the array.

Since prethinned silicon wafers cannot withstand the vacuum from the chuck spinner, the wafer must be isolated from the vacuum to prevent breakage. Figure 7 shows the aluminum disk used for this purpose.

A hot plate is used to softbake the polyimide. It is very important to keep the surface temperature of the hot plate below 100°C to avoid partial imidization of the polyimide that leaves resulting residues after development. Although an oven can be used for the softbake, it takes much longer (65° for 30 min).

The procedures for processing the polyimide are summarized in Table 3.2.

3.4. Metalization

The substrate is subjected to an oxygen plasma [Ficht, 1987] for three minutes to roughen up its surface. A thin layer of titanium is evaporated on the substrate followed by a layer of approximately 600 nm of gold. Theoretically, a monoatomic layer of titanium is sufficient.

Table 3.2

Polyimide Coating

1. Prepare the belt furnace (located in the undergraduate hybrid circuit laboratory in the Everitt Laboratory Building) for a six hour baking schedule with a peak temperature of 400°C. For our equipment this is achieved by a belt speed setting of 15 and temperature setting of 200°, 275°, 400°, 375°, 275°, and 200° for zones 1 to 6, respectively.
2. Using the aluminum disk to support the wafer, spin on diluted adhesion promoter AP3 [E.M. Industries, Hawthorne NY] (10 drops of AP3 in 5 ml DI + 95 ml isopropyl alcohol, IPA) at 4000 rpm for 30 seconds, followed by a 5 minute bake at 180°C. The diluted solution has a shelf life of 3 days.
3. Cool the substrate and apply Selectilux HTR 3-100. Slowly ramp up the spinner speed to 4500 rpm and spin for 30 seconds.
4. Softbake the substrate on 100° C hot plate for 2 minutes.
5. Expose under the Kasper aligner for 45 seconds with the perforation mask.
6. Develop the Selectilux by spray development
   a. spin the wafer on the chuck spinner at 2000 rpm.
   b. while the wafer is spinning, use a squirt bottle, positioned very close to the wafer, and spray the diluted developer D2 [E.M. Industries] (9:7 D2:IPA) on the center of the wafer for 15 seconds.
   c. without interrupting the spraying action, initiate spraying of both developer and IPA on the wafer for 10 seconds.
   d. continue spraying with IPA only for 10 seconds.
   e. spin dry: increase the spinning speed to 3000 rpm and spin dry for 30 seconds.
7. Postbake at 150°C for 80 minutes.
8. Cure the Selectilux in the belt furnace (see step 1).

The metal is patterned photolithographically by using PR, the conductor mask, and the mask aligner. A potassium iodide solution is used to etch the gold, and a hydrogen fluoride solution is used to etch the titanium. Care must be observed to prevent over-etching. The step is monitored by alternately etching and examining the progress under the microscope to determine the end-point.

The process steps for metalization are listed in Table 3.3.

Table 3.3

Metal Patterning

1. Subject the substrate to a 3 minute, 600 watt, oxygen plasma etch in the plasma etcher [Texas Instruments] located in the clean room in the Everitt Laboratory.
2. Evaporate titanium using 300 A of current for 30 seconds.
3. Without breaking the vacuum, evaporate the gold for two and a half minutes at 225 A at a substrate-source distance of approximately 10 centimeters. This will yield 600 nm of gold.
4. Spin on PR at 3500 rpm for 30 seconds making sure that the vacuum is isolated with the aluminium disk holder to prevent wafer breakage.
5. Softbake at 90°C, 20 minutes.
6. Expose the wafer under the conductor mask for 40 seconds.
7. Develop the PR pattern.
8. Hardbake at 110°C for 15 minutes.
9. Etch the gold for approximately 3 minutes (80 g KI, 20 g I_2, and add DI to 450 ml). Monitor the developing progress under the microscope.
10. Etch the titanium in 1% HF.
11. Rinse with DI and bake dry.

3.5. Insulation

Selectilux is applied as described in the polyimide coating section but adhesion promotor is not needed. The polyimide is photopatterned using the insulation mask and the steps in Table 3.2. A thicker layer of polyimide (DuPont Pyralin 2555) is applied by hand over the spun-on layer after the postbake to better protect the conductor patterns. The manufacturer suggests that once Selectilux is cured, it should not be subject to any temperature higher than at which it was cured. Thus, the curing temperature is reduced to 350°C. For the belt furnace, the new temperature settings are 200°, 270°, 350°, 350°, 250°, and 200° for zones 1 through 6, respectively.

3.6. Wafer Etching

The HF-HNO_3 system (25:15:60 HF:HNO_3:Acetic acid) [Schwartz and Robbins, 1976] is used to etch the wafer. Two factors help define the geometry of the hole in the wafer. First, a thin layer of oxide still exists and serves as a mask for a short period of time. Second, only a thin layer of silicon in the cavity remains. It can be etched completely before a substantial amount of silicon outside of this area is etched. A thin layer of oxide exists on the front side as well. Thus, after the wafer appears to have been etched through, some time is needed for the acid to dissolve the oxide.

A procedure follows for determining when the front side oxide has been removed. Use a piece of kimwipe to gently touch the perforated area. The polyimide is free of oxide when the kimwipe absorbs the liquid from the other side. A special setup (Figure 8) allows the acid mixture to come in contact with the center of the wafer only. It prevents the acid from attacking the polyimide film-wafer interface on the wafer edge, which can cause the polyimide to lift off.

An alternate procedure which protects the front side from accidental etching requires that the wafer be placed face down and its edge sealed to a glass plate with black wax (Figure 9) before the backside etch is performed. Upon completion, the black wax can be removed by trichloroethylene. This step can eliminate the acid attack on the polyimide-wafer interface completely.

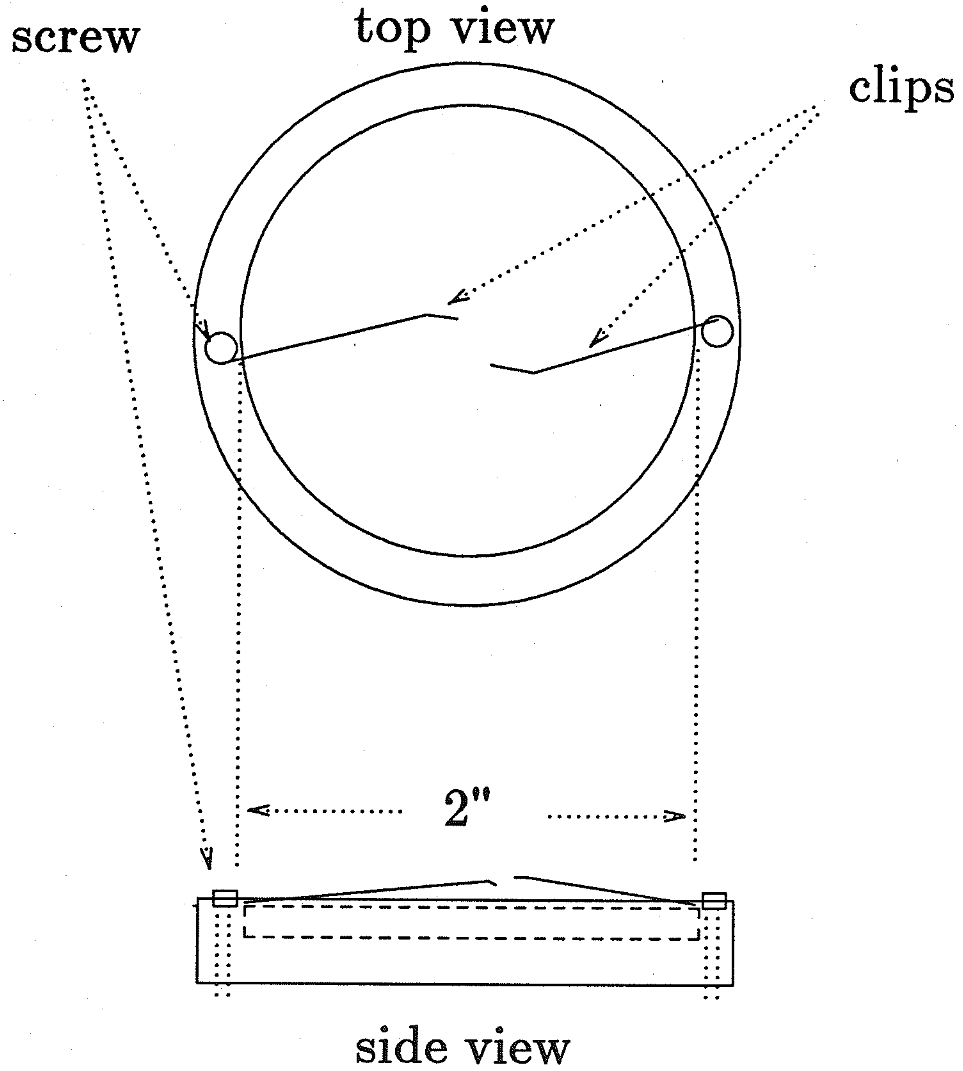


Figure 7. An aluminum disk with clips which is used to hold the wafer.

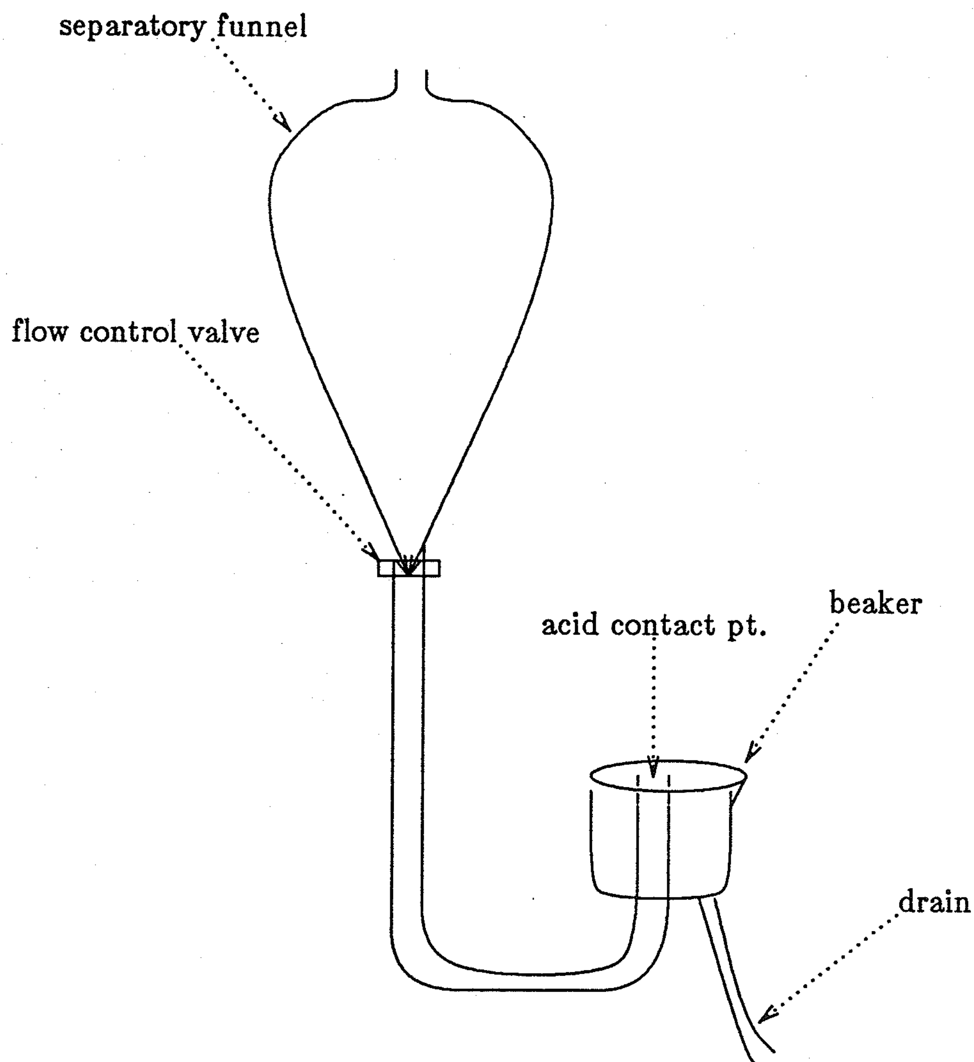


Figure 8. In this setup the wafer is placed on the beaker. The acid drips through the 1/4" diameter funnel and contacts only the center of the wafer. The acid is collected in the beaker and drained away through the small tube.

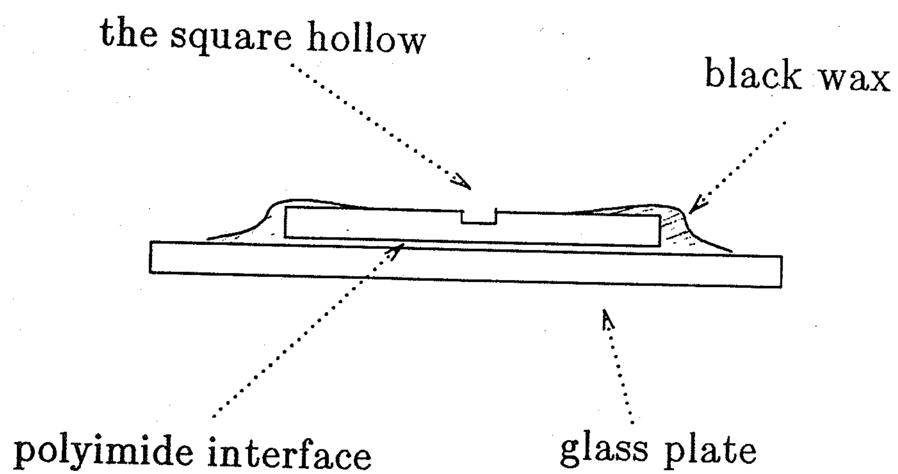


Figure 9. A cross-section sketch of the device sealed with black wax.

3.7 Electrode Plating

Plating electrodes with platinum reduces the impedance significantly. The plating is done by placing several drops of plating solution (3% platinum chloride and 0.025% lead acetate in 0.025 N HCl) at the electrode, and then passing a current of 1 to 3 microamperes for 30 seconds. This step must be done under the microscope.

At times a gas bubble will form around the platinum deposit indicating the reaction is proceeding too fast and that the plating current is too large. In this case, gentle application of a fine brush can remove the bubble.

Figure 10 shows the cross section of the device after completion of each major step.

3.8. Mounting

The device can be connected to external amplifiers through a ribbon cable via zebra connector strips (Tecknit, Cranford, N. J.). A zebra strip is composed of alternating layers of conductive (carbon filled) and nonconductive silicone rubber. Typical connection resistance for the zebra strip is 500 to 2500 ohms, and typical insulation resistance is 10^{12} ohms. The typical resolution is 100 conductive layers per inch. A reliable contact is maintained by applying a little pressure on the strips. The cable lead insulation is abraded on one side, exposing the copper conductors for contact to the zebra strip, while preserving the plastic on the other side for the integrity of the cable, and the onto the cable to form a socket to adapt the zebra strip. The

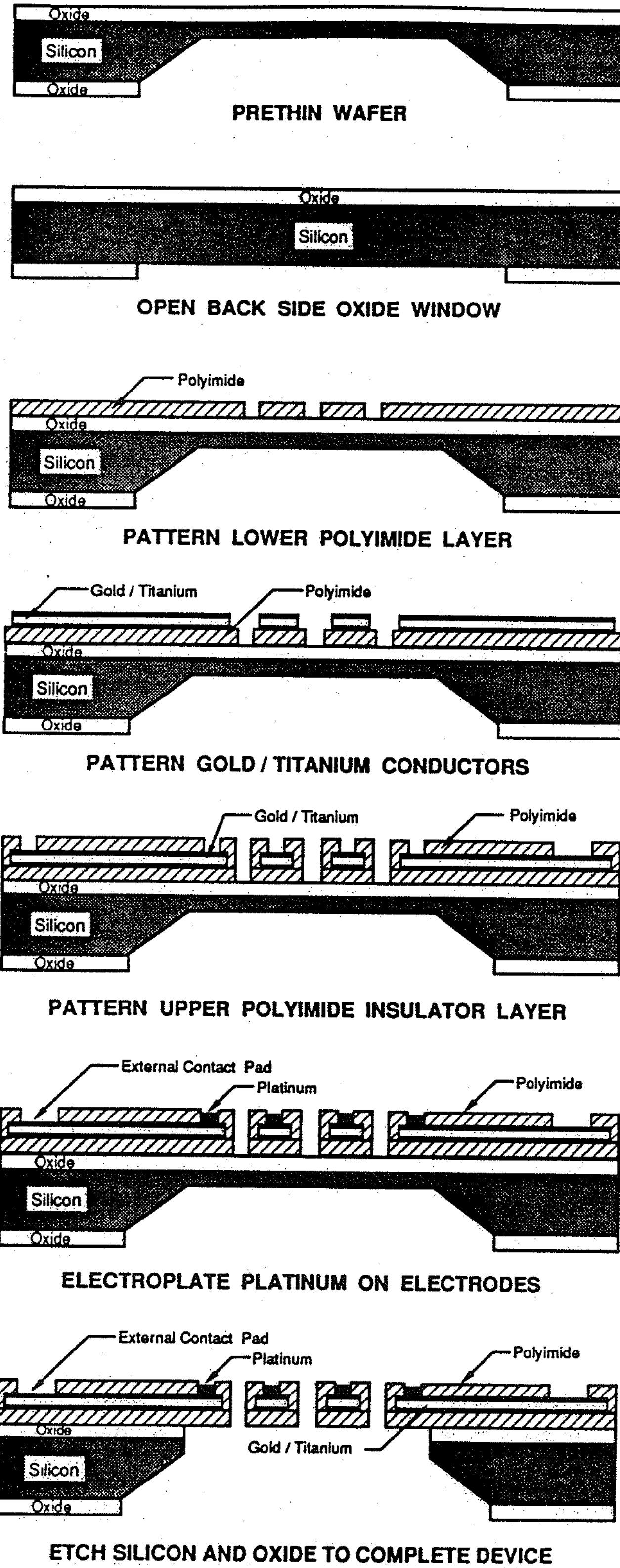
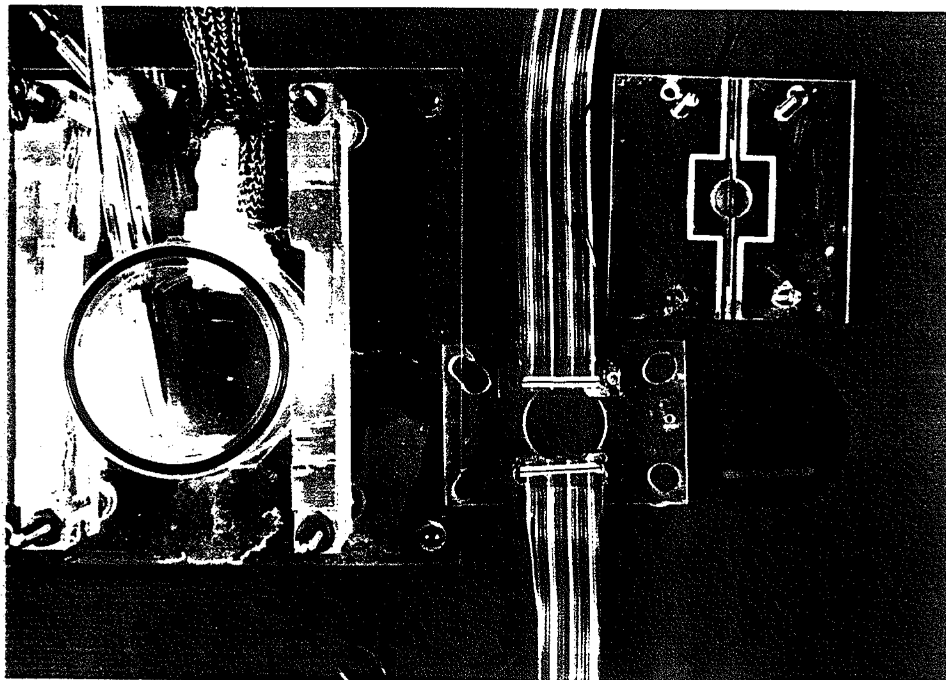


Figure 10. Device fabrication schedule.

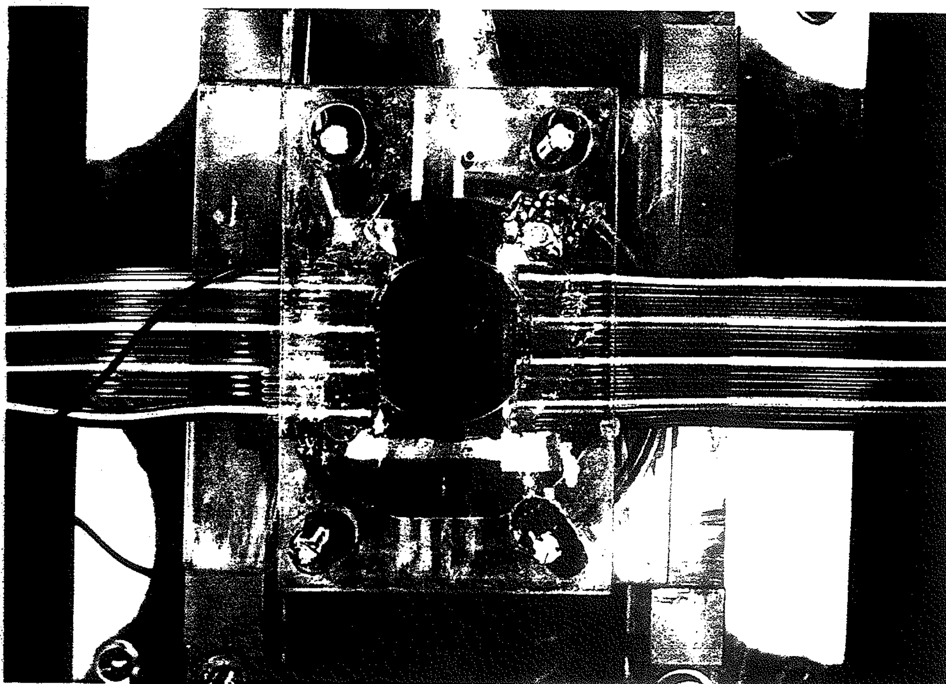
strip. The cable itself is glued onto a piece of plexiglas. The above assembly forms the top.

The base is a three inch square piece of plexiglas with three groves. The middle track is used as the saline solution canal. The two side tracks are filled with wax, and along with a sheet of parafilm, form a gasket between the device and the base to prevent leakage of saline solution. The device is sandwiched between the base and the top. Threaded rod and nuts are used to secure the assembly and to ensure good electrical contact between the device via the compressible zebra strip.

The physical assembly is shown in Figure 11.



(a)



(b)

Figure 11. The physical assembly of the recording chamber. In (a) are shown the unassembled components, including temperature controlled water bath (left), lower chamber directing saline flow (upper right) electrical connector (center), and wafer (lower right). The assembled chamber is shown in (b).

CHAPTER 4

ALTERNATIVE PROCEDURES

4.1. Introduction

In this chapter, three major alternative procedures are discussed. The first uses a nonphotosensitive polyimide, the second involves the use of reactive ion etching, and the last uses silicon nitride. Their advantages and disadvantages are discussed in Chapter 5.

4.2. The Pyralin Approach

Preliminary work was done using DuPont Pyralin 2555 polyimide and a preexisting mask set used to produce the earier planar array on glass substrate. This polyimide is not photosensitive, thus requiring extra processing steps, but it appears to be sturdier than Selectilux. This process was developed to obtain experience before commitment to the mask set described in Chapter 3.

The first step, the wafer prethinning, was the same as the one described earlier (Table 3.1).

4.2.1. Polyimide coating

The perforated polyimide film can be fabricated by following the insulation process described by Novak [1985] with a modified mask (Figure 12). The result is a layer of polyimide with the 4 x 8 electrode tip holes in the center of the wafer. These will be the perforations. The procedure involves spinning on a layer of

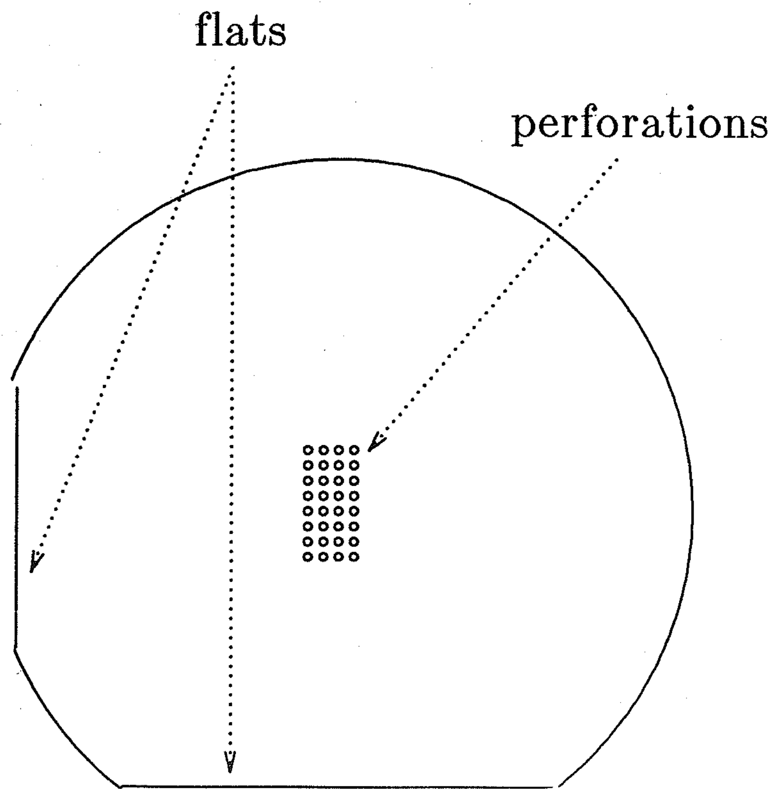


Figure 12. A dark field version of this pattern was used to pattern the Pyralin perforations.

polyimide (Pyralin 2555), photopatterning, and fully curing it. The thickness of the film is approximately 2 - 3 mms.

Table 4.1 summarizes the procedure.

Table 4.1

Pyralin Film Construction

1. Clean and bake dry the wafer.
2. Use the aluminum disk shown in Figure 5 to spin the following:
   a. adhesion promoter (1 drop of VM651 [DuPont] in 5 ml DI + 95 ml methanol at 4000 rpm for 30 seconds.
   b. DuPont Pyralin 2555 at 3000 rpm for 30 seconds.
3. Bake at 90°C for 10 minutes followed by 110°C for 10 minutes.
4. Spin on PR at 3500 rpm for 30 seconds.
5. Bake at 90°C for 20 minutes.
6. Expose under Kasper aligner with the insulation mask (Figure 11) for 40 seconds. Then cover up the center and expose the edge.
7. Develop in developer for approximately two and a half minutes. Examine under the microscope periodically, and terminate the process when the holes are etched completely through.
8. Strip the PR in 3:2 n-butyl acetate:IPA solution. Blow dry.
9. Cure the polyimide by one of the following methods
   a. on a hot plate: slowly ramp the temperature to 350°C over 45 minutes, allow the polyimide to cure at 350°C for an additional 45 minutes, then allow the substrate to cool down slowly.
   b. using the belt furnace to cure for one and a half hours [belt speed setting at 30], for a maximum temperature of 350°C [temperature setting for zones 1 to 6 of 200°, 300°, 350°, 350°, 350°,and 200°.

4.2.2. Wafer etching

In contrast to the preceding procedure, the backside etching is carried out before the metal evaporation, instead of as the final step. The procedures described in Section 3.6 are followed.

4.2.3. Metal patterning

This step is similar to the metal patterning section in Chapter 3. Although alignment is required, no alignment marks existed

in the old mask set. The alignment strives to stagger the perforated holes in between the electrode array.

4.2.4. Insulation

The insulation process is almost identical to the procedure developed by Novak [1985]. The variation here lies in the perforated holes and bonding areas for external connection.

In addition to the PR mask for electrode tip deinsulation, the perforated holes need to be etched through as well. Conveniently, the layer of fully cured polyimide can fulfill the role of a mask. During development, the partially cured polyimide is attacked from both sides. Since perforations are deeper than the tip holes and require longer developing time, when the tip holes are completely developed, the developing process is stopped to avoid overetching. The development of the perforated holes is continued by spraying the developer with a squirt bottle on the backside of the wafer. The wafer is examined under a microscope to confirm that the electrode tips are free of polyimide and that the perforations extend completely through the polyimide. The contact area for external connections is created by exposing the edge of the wafer to UV light, with the result that upon development of PR, the polyimide will have been removed.

4.2.5. Mounting

To utilize existing hardware, the two inch wafer was mounted on a three inch glass plate in a manner so that the saline solution will pass through the perforated holes. Two microscope

slides were glued to the three inch base plate creating a canal betweem them. The device was then glued on to the microscope slides as a bridge. The electrical path to the amplifiers are lines drawn by hand using paint-on-silver. The final insulation material tested includes epoxy, super glue, and Pyralin 2555. Figure 13 shows the components and the configuration of the final device.

4.3. The RIE Test

It was found that the procedure above, in which wet etching was used to pattern the Pyralin array, resulted in relatively poor control of the dimension of the holes. Therefore, reactive ion etching (RIE) was investigated as a means of obtaining better dimensional control. Although the additional complexity of the process made it less attractive than the photo sensitive polyimide process which was described in Chapter 3, in the future it may be desirable to reexamine this procedure for newer designs.

A preliminary test was done to determine the feasibility of RIE. Two layers of polyimide were spun on and cured in sequence in order to mimic the fabrication procedure. Spin on glass (SOG, Emulsitone Company, Whippany, N. J.) is spun on to the substrate at 2000 rpm for 30 seconds followed by a 200°C bake for two minutes, with a resulting 2000 angstrom layer of SOG. The SOG is patterned using PR and 0.5% HF.

The RIE is carried out in oxygen plasma. The sample is etched for a minute and then examined under the microscope. The process is repeated until the polyimide is etched all the way

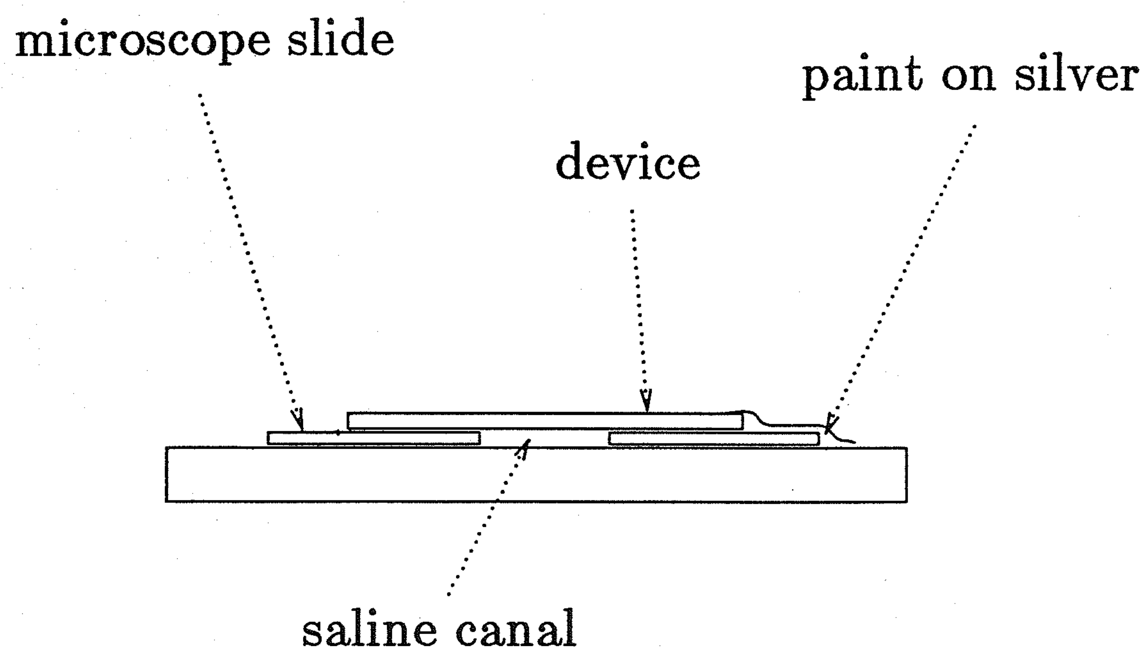


Figure 13. The physical assembly of the Pyralin device bridging over the microscope slide canal.

through. It was determined that a total of six minutes is needed to complete the etching process.

Reactive ion etching is a more desirable method, and as the early tests in RIE indicated, RIE is workable for our process. A suggested fabrication procedure using the RIE is described in Table 4.2.

Table 4.2

Suggested Fabrication Procedure Using RIE

1. Wafer prethinning:
   Follow the procedures described in Table 3.1.
2. Polyimide film generation:
   Follow the procedures described in Table 4.1, but do not pattern the polyimide, i.e., apply the polyimide, spin, and cure.
3. Metal deposition and patterning:
   Follow the procedures described in Table 3.3.
4. Insulation
   Follow the procedures described in Section 3.5, but deinsulate only the 4 X 8 electrode tips.
5. Backside etching
   Place the substrate on the funnel system and etch through the central window.
6. Spin on glass masking:
   a. Isolate the wafer from the spinner vacuum, and flood it with SOG solution (Silica film).
   b. Spin the wafer at 2000 rpm for 30 seconds.
   c. Cure the SOG on a 200°C hot plate for two minutes.
   d. Spin on PR at 3500 rpm for 30 seconds.
   e. Softbake, 90°C, for 20 minutes.
   f. Expose for 45 seconds with the perforation mask.
   g. Develop, and hardbake for 15 minutes.
   h. RIE the SOG in freon plasma; alternatively 0.5% HF can be used.
   i. Remove the PR with acetone.
7. Perforation
   RIE the wafer until the perforation holes are through, then dissolve the SOG with 0.5% HF.

4.4. Silicon Nitride

During the wafer etching step, the acid mixture often leaks through the polyimide-wafer interface and causes the polyimide film to lift off. In addition, the Selectilux film often breaks during this step. To solve these problems, silicon nitride (approximately 800 nm thick) coated wafers (supplied by Hewlett-Packard, Fort Collins, CO) were used in an attempt to isolate the polyimide film from the acid. The fabrication procedures described in Chapter 3 were carried out on wafers with the silicon nitride instead of silicon dioxide. The results from this brief investigation indicated that the quality and/or the thickness of the nitride were not adequate.

If an adequate nitride were obtained, it should be etched away using RIE with a gas mixture of 4% O_2 + 96% CF_4 after the device is completed. Had this solution been successful, the nitride would have been tested as the masking material for the perforations using the procedures described in Table 4.1, with the exception that the RIE mask is silicon nitride, and the RIE needs to be done with the device face down because the mask is at the bottom.

A preliminary investigation of low stress nitride (courtesy of Cornell University via Prof. I. Adesida; 170 nm thick) was also conducted. A free standing, perforated, silicon nitride diaphragm had been planned. The results of preliminary tests proved the nitride to be too fragile for the area it must span (7 mm X 7 mm). Thicker low stress silicon nitride, e.g., 300 nm, may be a viable alternative. In this application, nitride film can be

used as a substitute for the base layer polyimide, or it can be used in addition to the base layer of polyimide film.

The supply of the nitride was very limited, prohibiting any tests of its ability to isolate the polyimide film from the acid. This potential still appears to be promising.

CHAPTER 5
DISCUSSION AND CONCLUSIONS

5.1. Results and Discussion

5.1.1. Substrate creation

Since the overall procedure for etching the silicon substrate is quite cumbersome, it is appropriate to comment in more detail on the problems which limited the choice of procedures.

First, there is an incompatibility between the strong acids and bases used to etch silicon and the adhesion and integrity of the polyimide film. This is exacerbated by the fact that the entire thickness of the silicon wafer must be etched, eliminating RIE processing and requiring extended immersion of the substrate in the wet chemical etchants.

Once the polyimide film is applied, EDP and warm KOH are not suitable for etching the silicon wafer because they destroy the polyimide film. The alternative is to use the HF-HNO_3 system and etch the wafer from the backside. An acceptable masking material was not found. Black wax is the only material that can endure the time required to etch the entire thickness of the wafer, yet it cannot be patterned precisely and is awkward to use. The solution was to minimize the exposure time of the polyimide by prethinning the wafer and by setting it on the funnel system to avoid front side contact.

Additional obstacles include front to back alignment and the precision and resolution of the black wax masking pattern (black wax is melted and the pattern is painted by hand). Acid etchants

seep into the polyimide-wafer interface from both the outside edge and from the center cavity as it is etched through to the polyimide film. Finally, the etching pattern of this strong acid solution is inherently isotropic and proved difficult to control. The multistep etching procedure, combining isotropic and anisotropic etching steps, was chosen to overcome these limitations.

For the wafer thinning step, EDP was chosen over KOH because of its higher selectivity for etching silicon over silicon dioxide. Note that EDP is toxic; extra care must be observed when using it. Prethinning the wafer using a mechanical grinder was investigated but proved inadequate.

The difficulty in producing the substrate implies that there is great incentive to seek a means of producing the polyimide array separately from the processing of the substrate. The mechanically or chemically machined structures could be fabricated without concern for the effects of the processing on the finished array.

5.1.2. The negative polyimide approach

The selection of a light sensitive polyimide offered great advantages in processing. The first immediate advantage over the nonphotosensitive products is that no separate photoresist step is needed for photolithography. Additionally, it was possible to obtain far superior results in dimensional control of the polyimide perforations. The mask set (Chapter 3) was designed anticipating that the overetching would be so great that the square holes would appear as circles. The results (Figure 14) show that

a square profile can be preserved quite well even through a 3 mm thick polyimide film.

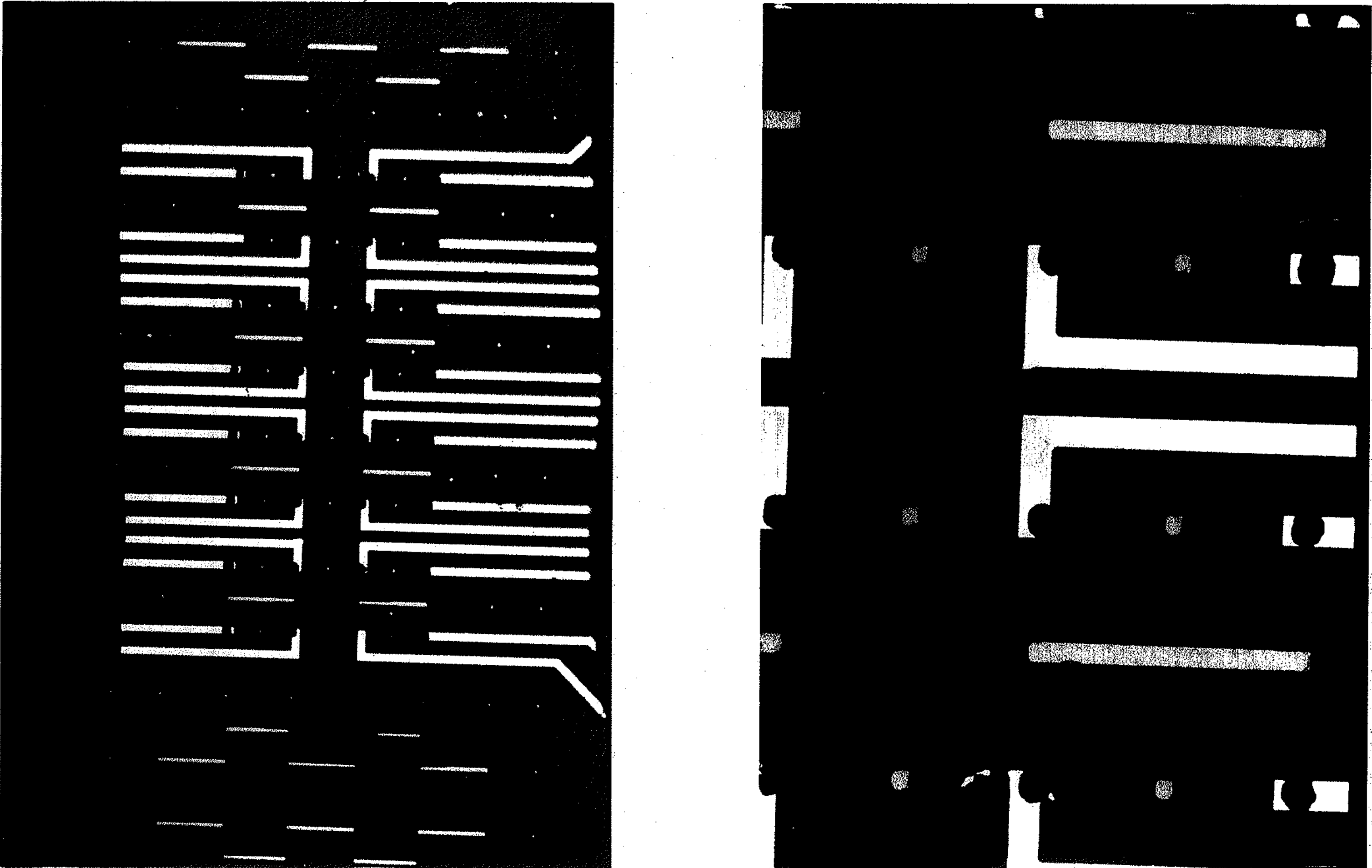
The Selectilux film was found to be more susceptible to breaking during the backside etching than the Pyralin. This would indicate Selectilux film is more fragile, although they are theoretically the same. Finally, the electrode plating can be performed repeatedly on devices fabricated using this method.

5.1.3. Preliminary invesigations with photo-insensitive polyimide

The preliminary device fabricated using this method turned out to be crude, partly because of the inadequate mask set and partly due to the poor dimensional control attained with the polyimide when patterned using an additional photoresist step.

The connections from the silicon wafer to its host three inch glass plate were not intended to be a permanent design solution. These proved to be inadequate, as indicated by the inconsistency in electrode plating from one trial to another. Thus, the silver paint is an unacceptable means of making a conductor over a step. Further, a suitable way to insulate the silver paint pattern was never found. Other connecting methods, including wire bonding and conductive epoxy, were insufficiently investigated to draw any conclusions.

The perforation holes crack often after the insulation layer of polyimide is cured. The cracking breaks the continuity of the electrodes and ultimately breaks the film. The breaks are likely



(a) (b)

Figure 14. These photomicrographs show the interior array pattern. For reference the platinum plated electrodes are 20 mm in diameter and separated by 200 mm. The holes between the plated electrodes are the perforations.

to have been caused by the etching solution in the deinsulation step [Dr. John Craig, DuPont, personal communication]. Despite attempts to control this, no solution was found and the problem is not understood. The Selectilux approach, however, did not have this problem.

Dimensional control of the etching of the Pyralin was very poor for the relatively thick layers needed. For 3 mm thick layers, overetching causes the holes to enlarge from the intended 25 mm to somewhere between 40 and 50 mms. This is not likely a problem with the DuPont product, but rather one common to the processing needed for any nonphotosensitive polyimide.

The fabrication procedure also calls for the free standing diaphragm to be made at an early stage. This results in a high accident rate for the remaining procedures and reduced yield. As mentioned in Section 5.1.1, there is significant incentive to decouple the array/film fabrication from the substrate fabrication.

Figure 15 shows a photograph of the device in which the cracking in the film is evident.

5.1.4. Reactive Ion Etching

This technique should be superior to wet etching for dimensional control of the etching of the perforation holes. However, dry etching does require prompt termination of the etching process or the underlying layer (gold in the electrode region) will be sputtered away.

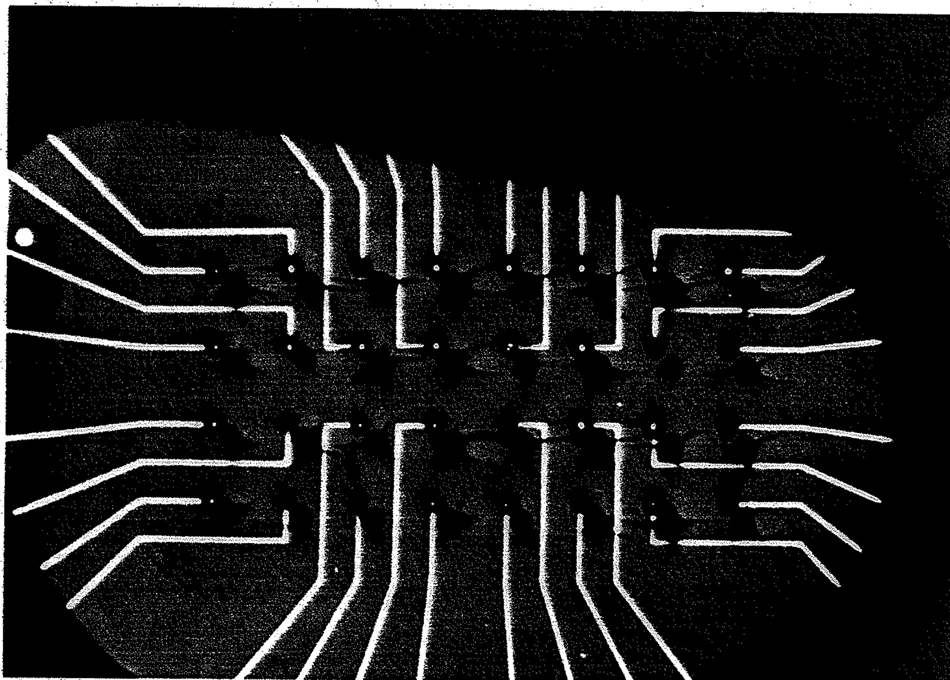


Figure 15. This photomicrograph shows the center of the Pyralin device. Note the cracking.

If the electrode tip and perforation holes are etched independently, then complete etch of the perforation hole no longer occurs at the expense of overetching the electrode tips. The RIE, however, is not appropriate for use in etching through the silicon wafer. Furthermore, acid can still attack the wafer-polyimide interface from the center once part of the hole is all the way through.

DuPont Pyralin 2555 is recommended for the base layer in place of Selectilux because it is less fragile during backside etching. The RIE testing also indicated that there is no adhesion problem between the two types of polyimide.

5.1.5. The recording setup

The devices fabricated using both methods were tested, and both showed that a saline solution can flow through the perforations from the canal. Preliminary attempts at measuring the electrical characteristics of the array resulted in unsatisfactory noise levels. However, this is likely due to the instrumentation external to the array.

Experiments with biological tissues are needed to determine if the perforations have prolonged the tissue life. These were not performed.

5.2. Potential Applications

It is possible to detach the entire polyimide film from the wafer. A flexible, perforated electrode array provides much flexibility for a recording technique. With such an array, one can

do recordings from the top (as well as the bottom) of the slice. One can even conduct a recording with an array-slice-array sandwich. Taking this idea a step further, one can conduct a recording with a series of planar arrays in a three dimensional sandwich to obtain three dimensional information.

The array can also be used for in vivo applications. Edell [1985] has developed a device for interfacing with regenerated axons of rabbit peripheral nerves. The design criteria for this device include a large number of microelectrodes (same order of size as the axons) to serve as contact area, perforations to allow regeneration of the nerves, and biocompatibility.

A flexible, perforated electrode array satisfies these criteria. In addition, the flexible array may be more favorable than Edell's design in two respects. First, the flexible array is less than 10 mm thick as compared to the 150 mm thick array in Edell's design. Furthermore, Edell's device is made out of silicon and is rigid. Upon implantation, it is likely to cause some trauma to its surroundings and induce the generation of the connective tissue. A flexible array is more likely to conform to its surroundings and move as the animal moves, thus reducing trauma.

5.3. Conclusions

A working procedure for fabrication of the perforated microelectrode array was developed during the period of this project. Recording from biological preparation is the next step in order to demonstrate the validity of the assumption that the perforated design can improve the health of neural tissues during recording.

The current methodology is functional but not optimal. Procedures which should improve the fabrication process were proposed, although the major improvement in the process is likely to lie in the direction of other choices of substrate and a process whereby the substrate processing is decoupled from the array processing.

A perforated, flexible, multichannel, microelectrode array offers much versatility. In addition to the hippocampal slice recording, it can be used in in vivo applications to sense the action potentials of a peripheral nerve or be arranged in a grid structure to gather three dimensional spacial information in a neural culture.

In summary, this project demonstrates the feasibility of a new technological approach to electrode array fabrication, and shows some exciting directions of neural science.

APPENDIX

SILICON OXIDATION PROCEDURE

The furnace is kept at a standby temperature. Approximately two to three hours before actual oxidation, set the center zone 1100^oC (dial setting 692) and allow the furnace to come to an equilibrium.

1. Bring furnace to temperature.
2. Cleaning the wafer:
   a. standard cleaning, acetone, IPA, followed by DI water rinse.
   b. soak the wafer in 20:1 DI:HF for 5 minutes.
   c. rinse (180 sec) and dry (180 sec) in the rinse-and-dry machine.
3. Load Wafers
   a. turn on the N_2 gas.
   b. remove the quartz carrier from the furnace.
   c. load the wafers into the quartz carrier, using a pair of clean, stainless steel tweezers. Be sure the front of the wafers (the shiny side) face the same direction. In addition, include 1 baffle wafer at each end.
   d. place the carrier in the elephant with the back of the wafer facing you.
   e. remove the endcap, and carefully attach the elephant to the furnace. Do not force fit the elephant. Slowly, push the carrier into the furnace until the mark on the pushing rod is at the furnace front panel level. Note: the front of the wafers should face you now. It is important not to push the carrier too fast as rapid changes in temperature can warp the wafers and make them brittle.
   f. administer the procedure according to the furnace cycle below.
   g. remove the elephant and replace the endcap.
4. When the oxidation is complete (3 1/2 hours), reverse the above and slowly pull the carrier to the elephant. Allow the wafer to cool in the elephant. The thickness of the oxide should be around 1.2 mm.
5. Shut down: turn off the gases, and turn down the center zone dial to the original position.

Furnace Cycle

Step	Time	Gases
Standby	-----	N_2
Push	3 min	N2, O_2Lo
Stabilize	3 min	N_2, O_2Lo
Dry Ox*	5 min	O_2Hi
Steam Ox	4 hr 25 min	O_2Hi, H_2
Dry Ox*	5 min	O_2Hi
Purge	3 min	N_2
Pull	3 min	N^2
Cool	5 min	N_2

* optional

Gas Flows

Gas	Flow Rate	Flowmeter Setting	Pressure
N_2	2.5 L/min	65.5 ss	20 psi
O_2Hi	2.5 L/min	72.4 ss	20 psi
O_2Lo	0.025 L/min	8.0 ss	20 psi
H2	2.09 L/min	34.7 gl	14 psi

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