# FABRICATION OF A SILICON BASED MICROELECTRODE

BY

PAUL ELWIN STEVENSON

B.S., University of Illinois, 1983

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 1985

Urbana, Illinois

# ACKNOWLEDGEMENTS

I would like to thank the people who have contributed to the completion of this thesis. First and foremost is my wife, Jane, without whose love and support I would never have attempted this work. Professor Bruce Wheeler suggested the topic of this thesis and advised me throughout the work. I appreciate the opportunity to observe his excellent research method and the extraordinary way he works with others. John Hughes maintains the laboratory where all this work was done and always took the time to answer my questions patiently, no matter what the topic. Wanda Elliott prepared this manuscript which has saved me countless hours. I am grateful she provides this service to graduate students. Finally, I would like to thank the Whitaker Foundation for providing the funding to support this work.

# TABLE OF CONTENTS

# CHAPTER 1

# INTRODUCTION

## 1.1. Background

The ability to record nerve signals detected with an array of precisely spaced electrodes will aid in the understanding of how information is encoded on a bundle of nerves. Nerve signals have been recorded since the 1930s, using single channel devices such as a glass micropipette filled with a conducting fluid or a single fine wire inserted into the animal. Multichannel devices are still in their infancy, although some sophisticated devices using integrated electronics have been developed [1].

Nerve signals can be detected as extracellular potentials. Placing a conductor near a nerve allows us to extract voltage waveforms that represent the action potentials of the many neurons present within a nerve, which constitutes a communication channel in an animal. In order to see how each neuron functions in the channel, it is necessary to place a detector near each neuron and record its activity when the animal is stimulated. Two ways to achieve this are to use a single recording device and move it from one axon to another or use a multichannel device and record the information simultaneously. A multichannel device has the advantage of giving precise information about the spatial distribution of the nerve signal.

To get precise spatial information, a multichannel device has several electrodes in an array. Since the spacing of the electrodes is known, the distribution of the signal through a region can be determined. There are three types of arrays.

Linear arrays have all the electrodes along a common line. Two-dimensional arrays have the electrodes distributed over an area. Three-dimensional arrays have electrodes distributed in such a way that information can be extracted from a volume of tissue.

It is desirable to mass produce the arrays. It allows more time for testing and actual recording. It also results in many identical devices which aid in data evaluation as slight device differences can color the data.

The geometry of the device should match the nerve tissue studied. A two- or three-dimensional array is well suited for nerves covering a large area such as brain tissue. Flat arrays can have tissue placed on top of them which requires partial or total removal of tissue from the animal. Probe type arrays are better for a long bundle of nerves, such as a spinal cord, where it is necessary to slip the device into the bundle. The electrode area should be large enough to reduce interface impedance, yet small enough to prevent recording from several neurons simultaneously.

The animal to be studied is the cockroach, which has 14 large neurons spaced approximately 35 $\mu$m apart. Electrode sites should be spaced accordingly. A probe type array is built so that the animal may be cut open and the device inserted. Probe tip thickness should be 10 - 20 $\mu$m to limit damage to the animal and 1 - 2 mm long to allow deep insertion. This eliminates the need for removal of tissue from the animal. The animal remains alive during the experiment so nerve signals can be generated by stimulating the animal.

A multichannel device can be as simple as a bundle of wires. Each wire will be an individual recording channel that hopefully will bring back information unique to its location. Linear [2] and two-dimensional [3] arrays of wire bundles have been used to make recordings. However, it is difficult to make a wire bundle with extremely fine dimensions. Signal processing circuitry cannot be incorporated into a wire bundle's substrate since it has none. Wire bundles are also made one at a time, which reduces the probability that electrode spacing is identical from one device to the next.

## 1.2. Materials

The microelectronics industry has solved the problem of making many small, identical devices at once. The techniques that allow this have been applied to many different electrode arrays [4]. The arrays can be divided into three regions: the substrate, the conducting lines and the insulator. Each requires a different material.

### 1.2.1. Substrate

The substrate should provide a strong insulating surface to support the conducting lines. It has to be compatible with the conducting line and insulator materials. Since a probe type array is to be built, the substrate should have the capability of being easily machined into thin beams. Ideally, electronics can be integrated into it for future signal processing circuitry.

May [5] built a probe with a sapphire substrate. It is strong and insulating, but his mechanical method of thinning the tip is limited to about 120 $\mu$m which is too thick. Molybdenum

has been employed by Kuperstein et al. [6] in making a probe which is thin enough. However, the conducting lines must be insulated from the substrate. The possibility of integrating electronics into the device is ruled out because the substrate is a metal. Wise [7] has built probes using silicon as a substrate. An insulating layer can be grown on the silicon, using simple equipment, and electronics can be integrated into it. The tip can be chemically machined into fine structures, and several etchants are available for doing this, the most common of which is an ethylene diamine-pyrocatechol-water (EPW) solution. Bohg [8] reports that EPW will not etch heavily boron-doped silicon as fast as other silicon. A thin beam can be formed by selectively doping the silicon in the pattern of the beam. The duration and temperature of the diffusion control how thick the tip will be.

### 1.2.2. Conductor

The conducting layer forms the communication channels and the electrode sites. It must provide a low impedance connection between electrodes and external recording equipment. Compatibility with the substrate and insulation layer is a necessity. The layers must adhere to one another. The conductor should be easy to deposit and pattern.

Picus [9] used a bimetal layer of gold on chrome. The chrome adheres well to silicon dioxide and gold adheres to chrome. Many different materials are suitable for insulating this conductor. However, the choice of insulation is limited because a low temperature process must be used when depositing the insulation. Photoresist is a suitable etch mask for gold.

Solutions of KI, $I_2$, and $H_2O$ will etch gold very rapidly [10]. The patterned gold layer serves as a mask for etching the underlying chrome, which can be etched with equal parts of HCl and glycerine [10].

Polysilicon is a reasonable choice of conductor. It is used in the electronics industry for interconnects and gates [11]. Its resistivity can be made small by doping, and many techniques are available for patterning it. Etching EPW requires a metal or glass mask [11]. Insulation can be carried out at either high or low temperatures, so selection of insulating material is not restricted.

Tantalum is another conductor that can be insulated at high or low temperatures and is easily deposited using electron beam evaporation. May [5] employed it in his device. Several techniques exist for patterning tantalum with etch solutions based on nitric acid. Tantalum has the advantage of having a native oxide that is both durable and insulating. This oxide is easily formed using an anodization process and can serve as an etch mask.

### 1.2.3. Insulator

The insulation layer must isolate the device chemically and electrically and be thick enough to reduce the shunt capacitance. It must also adhere well to the substrate and the conductor.

Photoresist will electrically isolate the device, but it is hydrophilic, so it tends to swell in saline solution. This changes the electrode site area, which must remain constant if the spatial distribution of the nerve signal is to be determined.

May [5] insulated his device with $Si_3N_4$. This provides an ion barrier, and nitride is a good dielectric. Nitrides are used as passivation layers in industry [11], so a wealth of information on working with them is available. Pine [12] reports using $SiO_2$ on a planar array. This is another good insulating layer that is easy to apply and pattern. A CVD reactor is necessary for their deposition.

Silicon monoxide and $Ta_2O_5$ have been used as dielectrics in hybrid circuit capacitors. Silicon monoxide can be applied by vacuum evaporation and is very chemically resistant. It can be patterned by a lift-off technique and adheres well to glass. Tantalum pentoxide is the native oxide of tantalum. May [5] uses it as a first layer of insulation and as a means to pattern his conducting lines. Solutions containing HF etch the $Ta_2O_5$ which is grown by passing a current between a platinum cathode and the tantalum anode.

## 1.3. Design Choices

The choice of material for a region of the probe is dictated by what chemicals and equipment are readily available. The University of Illinois has a fine microelectronics fabrication laboratory, which has hybrid circuit fabrication equipment in addition to the usual silicon processing facilities.

For the work reported here, silicon is used as a substrate. This is a natural choice considering the available facilities and wealth of material on silicon processing. Micromachining of silicon is commonly done in industry, so well defined procedures are available for defining the probe tip. All chemicals needed

are readily obtained.

Tantalum is used for the conducting layer because an electron beam evaporator is available for its deposition. Methods of patterning tantalum are reported in the literature [5], and the chemicals for doing so are found in a typical microelectronics laboratory. Unfortunately, lack of equipment prevented the use of polysilicon, which is another good choice of conductor.

Two different materials are investigated for use as the insulating layer. Initially, silicon nitride was to be used for all the work. However, when it became obvious that the CVD reactor used for its deposition would not become available until late in the work, an alternative material was sought. The equipment for evaporating silicon monoxide was on hand, so this material was put into service as an insulating layer. Fortunately, the CVD reactor did become functional so $Si_3N_4$ is also used as an insulating layer.

# CHAPTER 2

# METHODS AND MATERIALS

## 2.1. Procedure Overview

A set of masks was inherited, so probe outline, electrode size and spacing, and conducting line dimensions are all predetermined. The task ahead is to determine how to form the substrate, pattern the conducting lines, and insulate the device. Figure 1 gives a cross section of the desired structure.

Substrate formation is a two-step process. The first step is doping the silicon. Experiments are carried out to determine the proper diffusion time. Fair [13] has determined a profile for high concentration boron diffusions in a nonoxidizing ambient. Miin-Ron Lin et al. [14] have shown that boron diffusion rates are oxidation rate dependent. An oxidizing ambient is used for this work, so Fair's [13] profile is not appropriate. The second step is etching out the tip. Etch time and solution temperature need to be determined. Two different etch solutions are compared.

Determining an etch solution and etch mask are the main problems in forming the conducting lines and electrodes. Two different processes are attempted in order to find one which is consistent from batch to batch and is easy to perform. The processes differ in that one uses $Ta_2O_5$ as the etch mask and the other uses photoresist.

Experiments are done to determine the usefulness of $Si_3N_4$ and SiO as insulators. Methods of patterning them are determined, and their resistances to the tip etch are demonstrated.

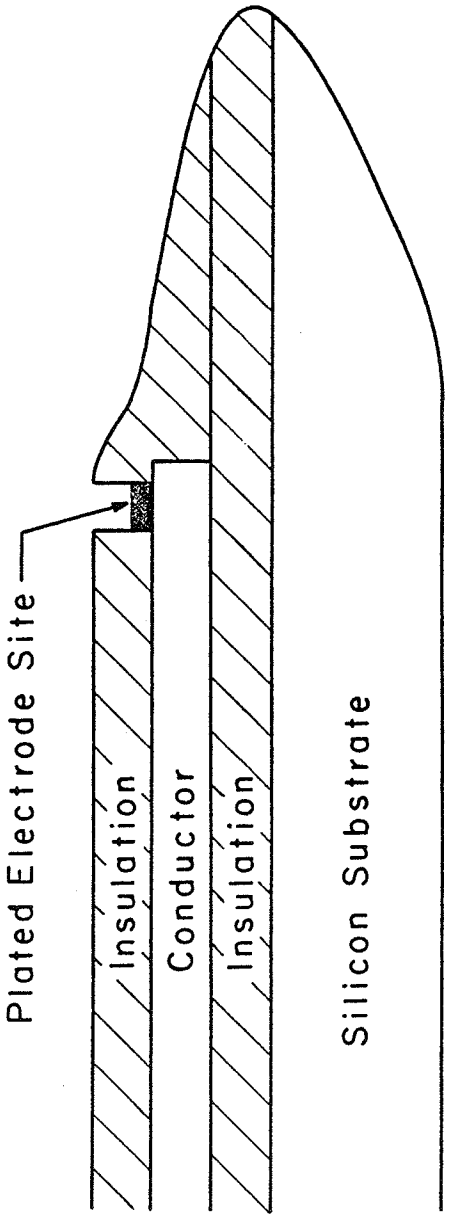



Figure 1. Tip cross section.

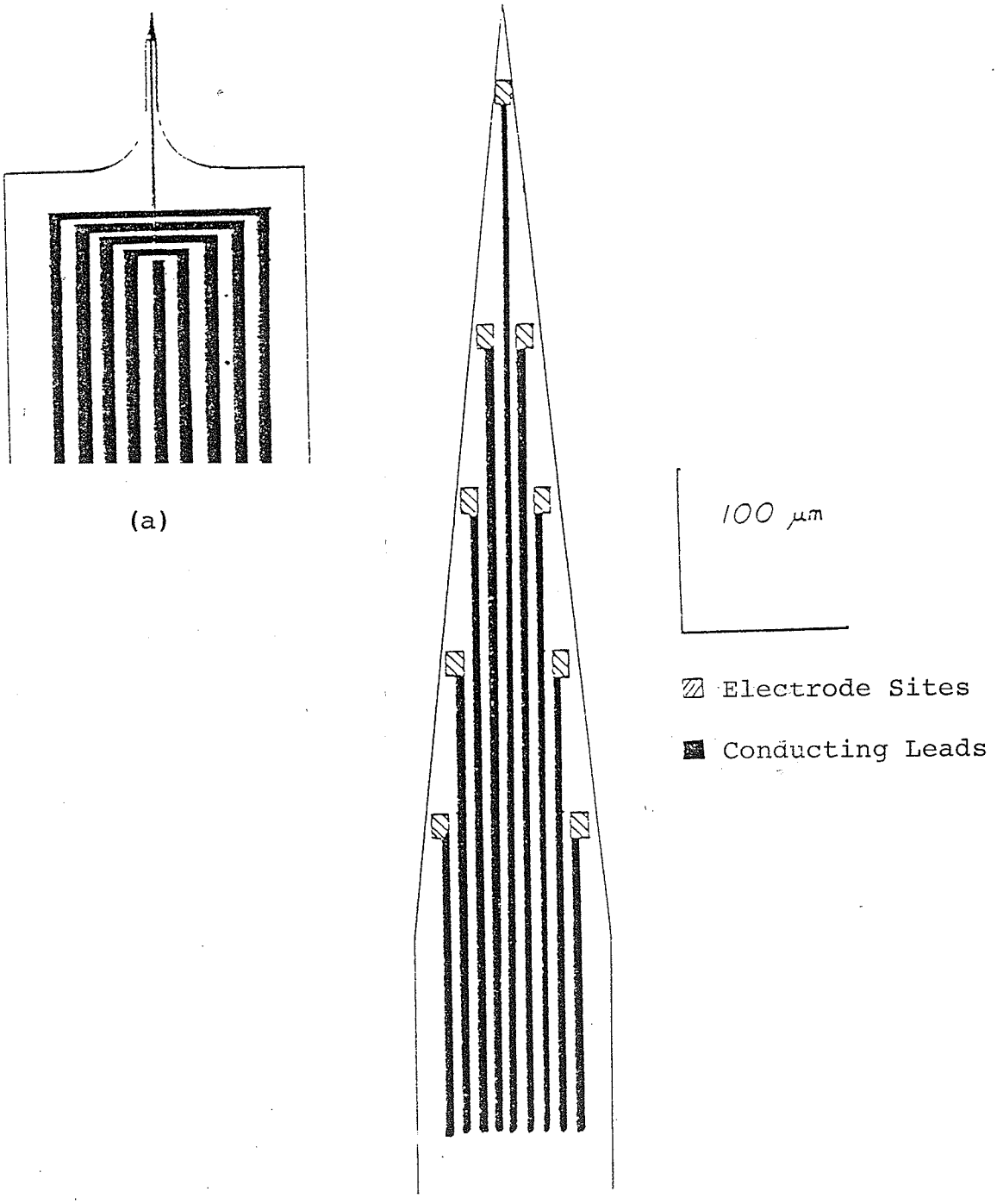
Platinum plating of the electrode sites is also attempted. The change in electrode impedance is measured to determine the effect of the plating.

A common goal of all the processes is that they be easy to perform. It is desirable to create a procedure that anyone can perform with a minimum of skills. This requires that each process be well characterized.

The masks provided define the probe area, conduction line pattern, and insulating layer. Figure 2a shows the probe outline, defined by the body mask, and the conducting lines which are defined by the conductor mask. The large conducting lines are 200 $\mu$m wide. The probe body is 1/2" x 1/4". Figure 2b details the tip of the probe. The electrode sites are spaced 75 $\mu$m apart running down the length of the tip. They are connected to 5 $\mu$m wide lines which lead to the 200 $\mu$m wide lines. The insulation mask is used to remove insulation from the electrode sites and most of the 200 $\mu$m wide lines.

### 2.1.1. Standard Photoresist

Three different photoresists are used, but the process is essentially the same for all three. Photoresist is applied to wafers that have undergone a cleaning process involving a 5 min rinse in acetone, a 5 min rinse in isopropyl alcohol, and a DI rinse to 10 M$\Omega$. If photoresist is to be removed from the wafer as part of the cleaning, a 5 min rinse in resist stripper precedes the acetone rinse. The cleaning is followed by a 20 min 120$^{o}$C bake-out to dry the wafer. Next, the wafer is flooded with the photoresist and then spun for 30 s at either 3000 or 6000




(a)

(b)

Figure 2. Neural probe design. (a) Top view. (b) Tip detail.

rpm. The choice of speed is determined by which photoresist is used; TF-20 and KTI 732 are spun at 6000 rpm, 1450J at 3000 rpm. The spin is always followed by a 20 min 90°C softbake. The wafer is then exposed to ultraviolet light through a chrome mask in contact with the wafer. The length of exposure is determined by the photoresist used and the dimensions of the pattern. Typically, 1 s exposures are used for the KTI 732, 19 s exposures for the TF-20, and 25 s exposures with the 1450J. The KTI 732 is always developed in KTI resist developer. A 1:1 solution of DI and Microposit resist developer is used for the two positive resists. Development is followed by a 20 min 120°C hardbake unless otherwise noted.

### 2.1.2. Wire Bonding

Aluminum wire bonding is used for all probes made. Two bonds are made for each channel on the device. One bond is made to the 200 $\mu$m wide tantalum lines. The other bond is made to the copper on the PC board on which the probe is mounted. An ultrasonic wire bonder is used for all the bonds made. Hughes' [15] thesis details the operation of the bonder used. The power and duration have to be determined for the tantalum bond and the copper bond, which is done by choosing a starting value for each and attempting a bond. If unsuccessful, the bond site is observed to see how damaged it is. The degree of damage is used to determine how the power and duration need to be adjusted.

Bonds are attempted on different thicknesses of tantalum to determine the minimum thickness of film necessary for a successful bond. Films from 1000 Å thick to 4500 Å thick are

used. The process is the same as above. No quantitative method is used to determine if a bond is too weak and, hence, the film too thin. Instead, a layer is deemed too thin if the operator cannot complete a bond before losing patience. This criterion fits the design philosophy of ease of construction.

## 2.2. Silicon Machining

### 2.2.1. Boron Diffusion

Boron diffusions of various predeposition and drive times are carried out to determine a diffusion process that results in tips approximately 10 $\mu$m thick. The first step is to grow an oxide mask against boron diffusion. The wafers used are 2" diameter (100) oriented p-type silicon. They are given a 15 s BHF etch followed by a 10 M$\Omega$ DI rinse prior to use. The mask oxide is grown in a steam ambient at 1100$^{o}$C for 4 hr. A 4 1/2" diameter furnace is used with $O_2$ flows of 3 1/2 l/min and $H_2$ flows of 2 1/2 l/min. This gives $SiO_2$ layers approximately 1.2 $\mu$m thick. A color chart is used for oxide thickness determination.

The oxide is patterned with the probe body mask. After the photoresist is hardbaked, the wafer is etched for 15 min in BHF followed by a DI rinse and the standard cleaning procedure.

All predepositions are carried out in a 3" diameter furnace using Carborundum Co. BN1250 wafers as the boron source. Prior to the predeposition experiments the four source wafers underwent a 15 min dry oxidation with an $O_2$ flow of 1 l/min at 1175$^{o}$C. The furnace temperature was calibrated once at the beginning of the work. The $N_2$ used as the carrier gas is boiled off from a liquid

$N_2$ source while all $O_2$ used is standard grade bottled gas. Wafers are placed into the hot furnace with little regard for crystal damage, as a slow push is not employed. Either a slow pull is used to remove the wafers or the furnace is allowed to cool to 400°C prior to removal. All drives are carried out in a 4 1/2" diameter furnace at 1100°C. A dry $O_2$ ambient is used with $O_2$ flows of 3.5 l/min.

A matrix of predeposition and drive times is used to experimentally determine the diffusion process that will give 10 $\mu$m thick tips. The carrier gas used is 1 l/min of $N_2$ and 50 ml/min of $O_2$. Twenty-four wafers were tested with predeposition times from 4 to 15 hr. Drive times from 2 to 18 hr are used.

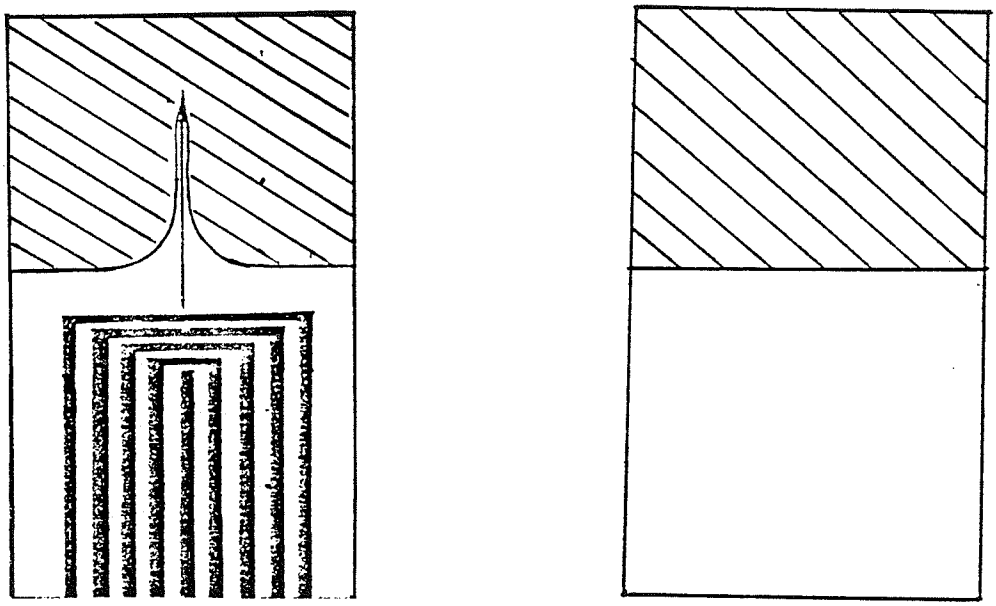
The diffusions must be profiled to find a predeposition and drive combination that will result in a 10 $\mu$m thick tip. Any predeposition and drive combination that results in a 10 $\mu$m thick tip is suitable. In order to profile the wafers, the tips must be etched free and a method of determining their thicknesses found.

### 2.2.2. Tip Etch

Experiments are done to determine an etch temperature that will result in a high percentage of tips which have a minimum of precipitate formation and are a uniform thickness down their lengths. The bulk of the experiments on etches is done with a 17 ml ethylenediamine, 8 ml water, 3 g catechol solution reported by Reisman et al. [16]. PSE-100, a hydrazine based etch (Transene Company Inc.), is also examined and its etch rate compared to that of EPW.

Etch experiments are conducted with the solution in three different states: a violently boiling solution, a gentle boil, and one in which the etch temperature is maintained at 100°C by placing the etch beaker in a large open container of boiling water. All etching is carried out in a 300 ml pyrex beaker fitted with a reflux chamber. Wafers are diced into 1/2" x 1/4" sections with each section containing one probe. The field oxide has been removed entirely from the front of the probe die, but remains on the backside except for the area directly beneath the tip. This leaves the body of the probe passivated on the front- and backsides of the die (see Fig. 3).

The teflon holder has five narrow slots evenly spaced around its perimeter that maintain a grip on the probes. The probes fit tightly in the slots with their tips vertical. The teflon holder, with dice in place, is put into a beaker with the etch solution at room temperature. The beaker is fitted with the reflux column, and the entire assembly is placed on a hotplate with the setting adjusted for the desired etch state. After 1 hr the probes are inspected every 15 min. Near the end of the etch, the probes are removed, rinsed with DI, and viewed through a microscope to see if the length of the tip is a uniform thickness. The tip is also inspected for precipitate build-up. The four variables recorded are the total time of etch, the overall appearance of the probe, precipitate formation, and the quality of the conducting lines. The data for two different etches are compared to see which etch solution to use and at what temperature.



(a) (b)

Figure 3. Probe prior to tip etch. Shading indicates where the oxide has been removed. (a) Top view. (b) Backside.

### 2.2.3. Tip Measurements

All probe tips are measured in the same way. Because they are so fragile, a mechanical profiler cannot be used. Instead, a microscope with an eyepiece micrometer is used. After a probe tip is etched free, it is placed between two slides on the microscope base so its edge is visible (see Fig. 4). The slides are placed tightly against the probe so that the probe is held perpendicular to the microscope base. The tip is viewed on the highest power objective lens available, typically giving 400X total magnification, for which the eyepiece scale is 10 $\mu$m/division.

### 2.2.4. EPW $P^+$ Silicon Etch

Since EPW is used to form the probe tip, it is desirable to know how rapidly it etches the heavily boron doped silicon. This rate will give an indication of how long a tip may be left in the etch without thinning it excessively.

The experiment done to determine the etch rate involves etching dice that contain probes. Since the probes are heavily doped, the dice contain a $P^+$ region and a less doped region. Six dice are etched in a beaker containing boiling EPW. The solution and setup are the same as that reported earlier for the tip formation. Three of the dice have been oxide etched so that they have no $SiO_2$ present on their entire surfaces. The other dice have the frontside oxide removed and the oxide from half of the backside removed. Figure 3 shows how the oxide remains on the backsides of the dice. The thickness of each is measured in two places: on the $P^+$ region and the low doped region. A micrometer

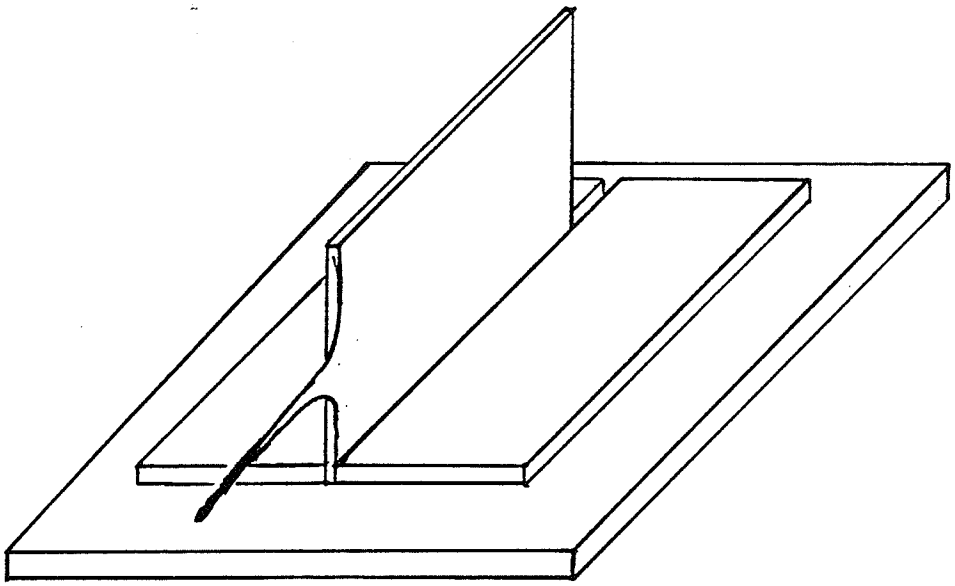


Figure 4. Microscope base with probe.

is used for all measurements and has an accuracy $\pm 1\,\mu m$. After the thicknesses are measured, the dice are etched for 45 min in the EPW. After thoroughly rinsing them with DI, their thicknesses are measured once more. The change in thickness for each region is calculated for comparison.

## 2.3. Conduction Lines

This section describes the experiments performed to determine a reliable way to pattern tantalum. Five $\mu m$ wide lines must be reproduced in tantalum that is 4000 Å thick. Two methods of patterning the tantalum are attempted, both positive and negative photoresist processes. The smoothness of the silicon surface affects the patterning of the tantalum, so the oxygen content of the boron diffusion carrier gas is adjusted to see its effect on the silicon surface.

All tantalum is deposited onto the wafers by electron beam evaporation at $5 \times 10^{-6}$ Torr. A crystal oscillator monitor, which has recently been calibrated using a Dektak surface profiler, is used to infer film thickness.

### 2.3.1. The Negative Process

The negative process determines a method of conveniently patterning tantalum using KTl 732 and $Ta_2O_5$. The KTl 732 is used to mask the tantalum in order to selectively grow $Ta_2O_5$ on its surface. KTI 732 is applied to wafers coated with tantalum and patterned with the positive image of the conducting lines. The exposed tantalum is anodized in a solution of 1 part oxalic acid, 2 parts DI, and 3 parts ethylene glycol. The wafer is held by an alligator clip which contacts the film and is attached by a lead

to the positive supply side of a current source. The wafer is immersed into the electrolyte only up to the clip. A platinum wire inserted into the solution is attached to the negative side of the current source and serves as the cathode. Current is passed between the wire and the wafer which results in $Ta_2O_5$ being formed on the surface of the exposed tantalum. A voltage drop of 0.06 V/Å of $Ta_2O_5$ accompanies this growth. Wafers are anodized to a forming voltage of 40 V.

After anodization, the wafers are stripped of photoresist. The conducting line pattern is now visible as the anodized region. All anodized wafers are etched in a solution of 10:1 HNO3:HF which attacks the tantalum about 100 times faster than the $Ta_2O_5$. The backside oxide is protected from the etch by a coat of clear nail polish. A single wafer is placed in 50 ml of etchant in a 500 ml teflon beaker and is swirled. When the tantalum appears totally etched, the wafer is removed, thoroughly rinsed, and observed under a microscope. It is important that the 5 $\mu$m lines are intact and have not been excessively thinned. The spaces in between are observed to make certain all tantalum has been removed. If necessary, the wafer is etched for additional intervals of 10 s until patterning is complete. The time of the etch is recorded as is the quality of the pattern.

### 2.3.2. The Positive Process

The positive process uses positive photoresist as the etch mask and determines hardbake time and temperature and etchant components. TF-20 is used exclusively and is always spun on at 6000 rpm. The goal of the first experiment is to see whether the

photoresist can be hardbaked long enough to make it etch resistant. The temperature of the hardbake is kept constant at 120°C with duration of the bake varying. The second experiment ramps the hardbake temperature from 90°C to 150°C in 10°C steps. The temperature is allowed to stabilize for 10 min before being increased. The ramp is used to reduce plastic flow of the photoresist. The wafers are etched with the same etch used in the negative process. Hardbake time, line quality, and ease of etching are recorded for comparison.

After the length of time for the 120°C hardbake is determined, the etch solution is altered. The acid components and their ratio to one another remains the same, but water is added to produce an etch that retains a high tantalum attack rate yet has a low attack rate on photoresist.

Wafers hardbaked at 120°C for 1 hr are used. The procedure is the same as above except etch solutions of 10:10:1 DI:$HNO_3$ and 5:10:1 DI:$HNO_3$:HF are used. The etch rate for each is recorded as is the attack rate on the photoresist. The ease of etching is noted, and these results are compared to the other methods used.

### 2.3.3. Oxygen Effects

The effect of oxygen during the boron diffusion on surface smoothness is examined. An attempt is made to pattern the tantalum deposited on wafers which have been boron doped with only nitrogen for the carrier gas. The surface smoothness is only a concern if it prevents patterning of the conducting lines.

Wafers are boron doped with 1 l/min $N_2$ for the carrier gas. Tantalum is deposited on them and the positive process is used to

pattern them. The quality of the lines is noted with particular attention paid to the 5 $\mu$m lines, as these are the most difficult to pattern. The results are compared to those for wafers doped in an $N_2$ plus 5% of $O_2$ ambient.

## 2.4. Insulator

Silicon monoxide is the first insulation layer examined. Experiments have the purpose of determining its resistance to EPW and finding a way to pattern it. A method of patterning $Si_3N_4$ is determined and the effect of its deposition on tantalum examined.

### 2.4.1. Silicon Monoxide

Four experiments are done with SiO. The first is to subject a layer to the EPW and measure how much etches away. The next two, back etching and lift off, are done to determine a suitable method of patterning SiO. Finally the complete probe structure, patterned tantalum on the substrate with SiO deposited on top, is subjected to the etch to determine if SiO will adhere to tantalum.

All SiO layers are deposited by vacuum evaporation carried out at $5 \times 10^{-5}$ Torr. An open crucible is filled with SiO powder, and 200 amps pass through it to evaporate the SiO. Two wafers are placed approximately 3" above the source. A crystal oscillator monitor which was not calibrated by this researcher is used to infer film thickness. A growth rate of 0.3 $\mathring{A}$/Hz is given. All wafers are cleaned prior to deposition unless they have photoresist on them.

2.4.1.1. Etch Resistance

A virgin (100) p-type 2" silicon wafer is diced into six pieces and then oxide etched and DI rinsed to 10 MΩ. SiO approximately 1300 Å thick is deposited on each piece. Five of the pieces are placed in a 900°C furnace with an oxygen ambient for 20 min. The sixth is not annealed in order to see if annealing is necessary. The backsides of the pieces are cleaned with a cotton swab dipped in HF. Aluminum of unknown thickness is deposited onto the backs of all pieces. The capacitance of each piece is measured using a mercury column capacitance meter to give an indication of SiO thickness. The pieces are etched for 1 hr and 40 min in boiling EPW, then removed and thoroughly rinsed in DI. The backside of each is cleaned with HF and aluminum is deposited. The capacitance of each is measured as before. The percentage change in the two values of capacitance for each piece is an indication of the change in thickness of the SiO layer.

2.4.1.2. SiO Patterning

After it is determined that SiO will survive the tip etch, a method of patterning is found. Back etching involves depositing a layer of SiO and then etching it to the desired pattern. Lift off has the SiO deposited on top of the patterned photoresist. When the photoresist is etched off, the SiO on top of the photoresist is also removed. A negative of the photoresist pattern is left behind in the remaining SiO.

One attempt at back etching is made. Silicon monoxide 2000 Å thick is deposited on top of a wafer that has been doped

and had the conducting lines formed. Photoresist is applied to the SiO and patterned with the insulation mask. After hardbaking at 120°C for 1 hr, the SiO is etched in a 1:1 $HF:HNO_3$ solution. The results are recorded.

The two experiments with lift off differ in that one has the wafers attached to a large copper heat sink during SiO deposition and the other does not. Wafers that have been doped and had tantalum applied and patterned are used. A negative of the insulation mask is used to pattern the photoresist which is not hardbaked. Silicon monoxide is deposited to thicknesses of 2000 and 5000 Å. The wafer is then placed in hot Posistrip to remove the photoresist and the SiO on top of the photoresist. The results are compared to determine whether a heat sink is needed during deposition.

2.4.2. Silicon Nitride Experiments

A cold wall reactor is available for depositing $Si_3N_4$ and $SiO_2$. A suitable method of patterning the two layers must be determined. There is a possibility that tantalum will react with oxygen during the high temperature deposition. Because this could change the characteristics of the tantalum, it is necessary to find a sequence of layers that will prevent the tantalum from reacting with any of the insulation.

Five experiments are done. Two of them compare different methods of patterning the $Si_3N_4$. One uses a dry etch technique and the other is a wet etch. The third is done to determine the effect that $SiO_2$ has on the tantalum during deposition. The fourth tests the tantalum in the $Si_3N_4$ wet etch. The last tests

the $Si_3N_4$ in EPW.

2.4.2.1. CVD Procedure

The reactor consists of a 1" x 4" x 48" quartz tube with a quartz boat and graphite susceptor for holding the wafers. High intensity lamps are used to heat the susceptor, which has a thermocouple inside to monitor wafer temperature during deposition.

All gases are mixed in a manifold prior to entering the reactor tube. Rotometer flow tubes are used to monitor gas flows which are adjusted with needle valves. Electronic grades $SiH_4$, 5% in $H_2$, Coleman grade $CO_2$ and standard grade $NH_3$ are the reactant gases. Nitrogen is the carrier for $Si_3N_4$ depositions, and $H_2$ is used for $SiO_2$ depositions.

The same procedure is used for all layers deposited with only reactant gases, temperature, and duration of deposition varying. All $Si_3N_4$ layers are deposited with $SiH_4$ flows of 200 ml/min, $NH_3$ flows of 1000 ml/min, and $N_2$ flows of 38.8 l/min. Silicon dioxide layers are deposited using the same $SiH_4$ flow, $CO_2$ flows of 912 ml/min, and $H_2$ flows of 54 l/min.

Wafers are cleaned and loaded onto the susceptor, which is then placed in the reactor. Nitrogen is allowed to flow for 3 min to exhaust any oxygen that entered the reactor. The susceptor is brought to 775°C, which take 5 min, while the reactant gases are allowed to stabilize in the vent mode. Once the susceptor is hot, the reactant gases are allowed to enter the reactor until the desired film thickness has been deposited. The deposition rate for $Si_3N_4$ in the reactor used is 200 Å/min. The

reactant gases are shut off but the heater is left on for 1 min to ensure complete reaction of any residual gases. Two things can happen at this point, depending on whether or not $SiO_2$ is to be deposited. If it is not to be deposited, the heater is shut off and the susceptor is allowed to cool for 5 min before the wafers are removed from the reactor. If it is to be deposited, the carrier is switched from nitrogen to hydrogen. The hydrogen is allowed to flow for 5 min while the susceptor reaches 800°C. During this time the reactant gases, $CO_2$ and $SiH_4$, are allowed to stabilize while being vented. The gases are allowed to enter the reactor and $SiO_2$ is deposited at 100 Å/min until the desired film thickness is achieved. The heater is left on for 1 min after the reactant gases are shut off. Hydrogen is allowed to flow for an additional 3 min, then nitrogen is used to purge the reactor for a minimum of 5 min prior to wafer removal.

2.4.2.2. Dry Etch

Two types of wafers are used. One type is virgin (100) p-type silicon that is given a 15 s oxide etch followed by a 10 MΩ DI rinse. The other type has been doped for tip formation and has tantalum patterned with the conductor mask on its surface. The tantalum lies on top of 6000 Å of thermally grown oxide. This wafer is given the same cleaning procedure as the virgin silicon wafer. After the wafers are cleaned they have 2500 Å of $Si_3N_4$ deposited on them.

The wafers are allowed to cool and then are coated with 1450J. The photoresist is patterned with the insulation mask and hardbaked at 120°C for 20 min. A Tegal in-line plasma etcher is

used for all dry etching. The reactor chamber allows one 2" wafer to be etched at a time in a $CF_4$ plasma produced using 100 W of RF power at 1 Torr.

The virgin wafers are used to establish the etch rate of the plasma. A single wafer is loaded into the chamber which is then evacuated to 0.2 Torr. Freon is allowed to enter the chamber at a pressure of 1 Torr. The field is applied and the plasma established. The wafer is etched for 2 min, removed from the chamber, and examined to determine if the $Si_3N_4$ has been completely removed. The process is repeated until all unmasked $Si_3N_4$ is removed. The total etch time is recorded for future reference.

After the etch rate is determined, the tantalum processed wafers are etched. Ghandi [11] reports that $CF_4$ plasma will etch tantalum at approximately 100 Å/min. It is hoped that an etch time can be determined that will remove the $Si_3N_4$ but leave most of the tantalum intact. In order to do this the tantalum patterned wafers are etched in the same fashion as the virgin wafers. The color of the tantalum is noted after $Si_3N_4$ removal is complete. The tantalum is probed to determine conductivity.

One additional experiment is done to see the effects the plasma has on tantalum and $Ta_2O_5$. A wafer with tantalum and $Ta_2O_5$ on it is etched for 2 min. It is then removed from the etcher and examined. The changes in the tantalum and $Ta_2O_5$ are noted.

2.4.2.3. Wet Etching

The ability to pattern the $Si_3N_4$ with hot $H_3PO_4$ and its

effects on tantalum and $Ta_2O_5$ are studied. $SiO_2$ is used to mask the $Si_3N_4$ from the boiling acid. Four virgin (100) p-type silicon wafers and two wafers, which have been doped for tip formation and had tantalum deposited and patterned with the conductor mask, are used. The tantalum lies on 6000 Å of thermally grown $SiO_2$. The wafers are cleaned and have 2500 Å of $Si_3N_4$ deposited on them which is then coated with 1500 Å of $SiO_2$. This results in an insulation layer 4000 Å thick.

Once the wafers are cool, 1450J is applied and patterned with the insulation mask. The $SiO_2$ is then etched in BHF in 10 s steps. The wafer is etched for 10 s and then DI rinsed. The color is noted. The procedure repeats until no change in color is observed after an etch period. At this point the unmasked $SiO_2$ has been removed. The total time of etch is recorded. After the photoresist is removed using the standard clean, the wafers are ready for the boiling acid etch. The etch is done in a 300 ml pyrex beaker fitted with a reflux column. One hundred and fifty milliliters of 85% $H_3PO_4$ are added to the beaker and brought to a boil. A wafer in a teflon holder, that keeps the wafer vertical, is placed into the boiling acid. The wafer is removed and rinsed with DI after 10 min. The unmasked $Si_3N_4$ is observed and its color noted. The wafer is replaced into the acid. The procedure repeats until all $Si_3N_4$ has been removed. The total time of etch is recorded.

The effect the hot acid has on tantalum and $Ta_2O_5$ is observed with a qualitative experiment. A virgin silicon wafer has 2000 Å of tantalum deposited on it. The tantalum is patterned with the conductor mask and has been selectively

anodized to 1000 Å. This results in both tantalum and $Ta_2O_5$ being exposed on the wafer surface. The wafer is placed into 150 ml of boiling $H_3PO_4$ for 1/2 hr. It is then removed and rinsed with DI. The quality of the tantalum and $Ta_2O_5$ is recorded.

2.4.2.4. Layered Structure

A layered structure is built in another qualitative experiment to determine a structure that leaves the tantalum film unchanged after the depositions. The experiment is brief and is only intended to give a working process. No optimization is attempted.

Two (100) p-type silicon wafers are employed. One has 6000 Å of $SiO_2$ grown on its surface in a steam ambient at 1100°C. The other has 1500 Å of $SiO_2$ deposited on it using the aforementioned $SiO_2$ deposition process. Both wafers have 4000 Å of $Si_3N_4$ deposited on them at 800°C. They are removed from the CVD reactor, have 4000 Å of tantalum deposited on them, then replaced into the CVD reactor and have another 4000 Å of $Si_3N_4$ deposited at 775°C. The $Si_3N_4$ layer is followed by 1500 Å of $SiO_2$ deposited at 800°C. The total time required to deposit the two materials on top of the tantalum is 40 min.

The wafers are removed from the reactor and have their surfaces selectively masked with nail polish. The $SiO_2$ is then removed with a 30 s BHF etch. Once the nail polish is removed with the standard clean, the wafers are ready for the $Si_3N_4$ etch. The same setup is used as reported earlier. This time, however, the wafers are allowed to etch for 2 1/4 hr in the boiling acid. The wafers are removed and the tantalum inspected. A sheet

resistance measurement is made using a four point probe.

2.4.2.5. EPW Etch Resistance

Three wafers are placed into boiling EPW for 1 1/2 hr to see if the $Si_3N_4$ and $SiO_2$ can withstand it. One wafer used is a five layer structure. The substrate is a doped wafer with 6000 Å of thermal $SiO_2$. Tantalum lies on top and is patterned with the conductor mask. This is covered with a 2000 Å layer of $Si_3N_4$ which is coated with 1500 Å of $SiO_2$. The $SiO_2$ and $Si_3N_4$ have not been patterned. However, the film has peeled back exposing the underlying tantalum. The second wafer has four layers. It is the same as the above wafer with the exception that the deposited $SiO_2$ is omitted. This wafer was used in the plasma etching experiment, so the $Si_3N_4$ is patterned with the insulation mask. The tantalum at the electrode sites and bonding pads is exposed. The third wafer is a three layer structure. It consists of a virgin (100) p-type silicon wafer which has had 2000 Å of $Si_3N_4$ and 1500 Å of $SiO_2$ deposited on it. The $SiO_2$ and $Si_3N_4$ have been patterned with the insulation mask.

A 300 ml pyrex beaker has 51 ml of ethylenediamine, 24 ml DI, and 9 g catechol placed into it. The solution is brought to a boil. The three wafers are placed into the teflon holder and the entire assembly into the EPW. The EPW is maintained at a violent boil. After 1 1/2 hr the wafers are removed and thoroughly rinsed in DI. The wafers are observed to see if film lift off has occurred.

2.4.3. Electrode Impedance

There are two impedances of importance with the probe, the

electrode-saline impedance and the shunt impedance. The method of measuring them is the same for both and is described below. It is important to know the electrode impedance in order to determine how the impedance affects the SNR. This impedance is measured before and after plating the electrode sites with platinum in order to determine the effect of the platinum plating. The shunt impedance is measured using probes that have not had the insulation removed from the electrode sites. The shunt impedance must be much larger than the electrode impedance for a good SNR.

The test setup consists of a two channel oscilloscope and a high gain amplifier. A Wavetek, Model 190, function generator is used to produce the 1 kHz signal. A drop of physiological saline is placed on the electrode area of each probe and has a silver-silver chloride wire inserted into it. A 1 kHz signal of known amplitude is applied between one electrode on the probe and the wire. The current that passes between them is amplified and converted to a voltage which is displayed with the source voltage on the oscilloscope. The amplifier gain is known so the magnitude and phase of the electrode impedance can be determined from the two waveforms.

After their impedances are measured, the electrodes are plated with platinum. This is done to determine if platinum plating results in a reduction of electrode impedance. A drop of 3% platinum chloride and 0.025% lead acetate in 0.025 N HCl is placed on the electrode area of the probe and has a platinum wire inserted into it. A 1 $\mu$A current is passed between the wire and an electrode site for 20 s. This is repeated for all sites, and

they are checked through a microscope and their appearance recorded. The impedance of each site is tested once again. The two impedances, before and after platinum plating, are compared.

# CHAPTER 3

# RESULTS

In the following section the results of the experiments that were done to determine processes to form the probe are reported. Results for each region of the probe are reported in a separate section corresponding to the appropriate methods section of Chapter 2. Most of the data is contained in tables; however, some of the results are singular and are contained in the text.

## 3.1. Substrate Machining

The purpose of the substrate machining experiments was to determine a two-step process, doping and etching, that results in 10 $\mu$m thick tips. Table 1 contains the data for the first three wafers etched. More were not etched because the desired result was obtained with the third entry in the table. The third entry has a 1 hr drive that is used to grow 6000 Å of $SiO_2$ to insulate the conductors from the silicon.

The second step in the tip formation process is the tip etch. Two different etches were examined and the results are listed in Table 2. The silicon etch rates reported were determined from how long it took for a tip to etch free. This required etching through approximately 250 $\mu$m of silicon. The tantalum attack rate is a qualitative result. The PSE-100 etched all tantalum away before the tip was completely formed. The EPW, on the other hand, has essentially no effect on the tantalum or on $Ta_2O_5$. The layers were always as smooth upon removal from the etch as they were when they went in.

Table 1

Boron Diffusion

| Diffusion | Tip Thickness | Comments |
|---|---|---|
| 15 hr 1175°C predep<br>8 hr 1100°C drive | 20 μm | too thick, could damage animal |
| 4 hr 1175°C predep<br>18 hr 1100°C drive | <10 μm | too thin, curls 90° |
| 10 hr 1175°C predep<br>1 hr 1100°C drive | 10 μm | curls slightly |

Table 2

Etch Rates of Tip Etchants

| Etch Solution and State | Silicon Etch Rate | Tantalum Attack |
|---|---|---|
| PSE-100 violent boil | 40 μm/hr | rapid |
| EPW 100°C | 25 μm/hr | negligible |
| EPW violent boil | 50 μm/hr | negligible |
| EPW slow boil | 50 μm/hr | negligible |

The usefulness of the etchants cannot be determined from the tables. Of the three different ways that the EPW was used, only the third entry is useful. The 100°C solution results in extreme

precipitate build-up which makes wire bonding and platinum plating difficult. The violently boiling EPW breaks the tips off during etching. Attempts were made to baffle the solution by including oxidized silicon wafers sandwiched around each probe, but the solution was too turbulent. The slow boiling solution has negligible precipitate formation and does not break the tips. The PSE-100 etches tantalum negating its use.

### 3.1.2. EPW $P^+$ Silicon Etch Results

The results of the experiment done to determine the etch rate of the heavily doped silicon are in Table 3. Dice 1 - 3 have $SiO_2$ on their backsides, 4 - 6 do not. The column headings refer to the thicknesses of the P and $P^+$ regions before and after etching. The final column is the change in thickness of these two regions. The increase in thickness of die No. 2 lies within the margin of error of the measurement method and does not indicate an actual increase in thickness.

The qualitative results are of importance. Most notable is the appearance of the $P^+$ silicon compared to that of the less doped silicon. It was obvious that the low doped silicon had etched from the contours on its surface. These were not present on the $P^+$ silicon.

Table 3

EPW Etch of $P^+$ Silicon

| Dice No. | Before | | After | | Change | |
|---|---|---|---|---|---|---|
| | P $\mu$m | $P^+$ $\mu$m | P $\mu$m | $P^+$ $\mu$m | dP $\mu$m | $dP^+$ $\mu$m |
| 1 | 260 | 263 | 232 | 263 | -28 | 0 |
| 2 | 253 | 257 | 230 | 258 | -23 | 1 |
| 3 | 258 | 263 | 239 | 259 | -19 | - 4 |
| 4 | 257 | 260 | 220 | 236 | -37 | -24 |
| 5 | 160 | 258 | 229 | 237 | -31 | -21 |
| 6 | 259 | 255 | 234 | 234 | -25 | -21 |

## 3.2. Conductor Patterning

The conductor patterning experiments were done to find a reliable way of patterning 5 $\mu$m wide lines in tantalum films 4000 Å thick. The results of the experiments are listed in Table 4. The etch rates were determined by timing how long it took for the tantalum to etch completely away. Since the thickness of the tantalum layer is inferred from a crystal monitor, it is not precisely known. Therefore the etch rates are not precise. However, they are useful for comparison.

Table 4

Conductor Patterning

| Mask | Etchant | Etch Rate | Pattern Quality |
|---|---|---|---|
| 640 Å $Ta_2O_5$ | 10 $HNO_3$:1 HF | 4000 Å/min | good |
| 120°C hardbaked TF-20 | 10 $HNO_3$:1 HF | 4000 Å/min | poor |
| 150°C hardbaked TF-20 | 10 $HNO_3$:1 HF | 4000 Å/min | poor |
| 120°C hardbaked TF-20 | 10 $HNO_3$:1 HF 5 DI | 2700 Å/min | good |

The pattern quality refers to the ability to reproduce 5 $\mu$m wide lines. While it is possible to do this with all the methods used, only the first and last entries in Table 4 do so all the time. The other two entries can be made to pattern the tantalum by pouring a small amount of etchant on the wafer and gently agitating it. A large amount of DI must be kept close at hand to rinse the wafer the instant the tantalum has etched away. This is an unreliable method and results in many bad probes. The "good" entries exhibit no problem with their masks etching away.

The final result to report is that a 5% $O_2$ carrier is needed during the boron diffusion. If the oxygen is not present, the wafer surface is too pitted to pattern the tantalum. Addition of oxygen eliminates this problem.

## 3.3. Insulation

There are many results from the insulation experiments with the most important listed in Table 5. The first column lists the type of layer. The next three are concerned with patterning the layer. Since patterning the SiO and $Ta_2O_5$ did not require etching, no entries are included in columns 3 and 4 for these materials.

Table 5

Insulation

| Insulation | Patterning Method | Etchant | Etch Rate | EPW Etch Resistance |
|---|---|---|---|---|
| SiO | lift off | na | na | good |
| $Si_3N_4$ | back etch photoresist mask | $CF_4$ plasma | 500 Å/min | good |
| $Si_3N_4$ | back etch $SiO_2$ mask | 85% $H_3PO_4$ | 32 Å/min | good |
| $Ta_2O_5$ | selective anodization | na | na | good |

The EPW resistance listed is a qualitative result. If the layer effectively masked the silicon during the etch experiment, then its resistance is deemed good. The SiO etch rate was determined and is 60 Å/hr. Unfortunately, SiO does not adhere to the tantalum during the tip etch, so it is unsuitable for use as an insulator. One further comment about the SiO is that the 1 $HNO_3$:1 HF solution used to back etch it attacks the silicon and

$SiO_2$ very rapidly. Back etching is not a viable way of patterning SiO.

The plasma method of patterning the $Si_3N_4$ results in an altered underlying tantalum layer. The tantalum changes color and does not conduct when contacted with microprobes. These problems did not occur when using boiling acid to pattern the $Si_3N_4$. The acid had no visible effect on the tantalum or $Ta_2O_5$ after 1/2 hr of immersion.

The results of the experiment to determine a sequence of layers to be deposited on the wafer is that the tantalum should be sandwiched between layers of $Si_3N_4$. The resulting structure has five layers starting with the silicon substrate, a thermal oxide, a deposited $Si_3N_4$ layer, tantalum, deposited $Si_3N_4$ and finally deposited $SiO_2$ layer to pattern the $Si_3N_4$. The sheet resistance of the tantalum film after the deposited $Si_3N_4$ and $SiO_2$ were etched away was 13.5Ω/sq. This compares favorably with the sheet resistance of freshly deposited tantalum of 10.5Ω/sq.

## 3.4. Electrode Impedance

The results from the electrode impedance measurements are broken down into two sections, impedance measurements of working devices, and impedance measurements of totally insulated devices. The working devices are deinsulated on the electrode sites and have their impedances measured before and after platinum plating. The totally insulated devices have not been deinsulated and are used to determine the shunt impedance of the probes. The top side insulation lies on top of the tantalum while the substrate

insulation is between the tantalum and the silicon substrate. All measurements were done using a 1 volt zero-to-peak 1 kHz signal unless otherwise noted.

### 3.4.1. Working Devices

Many more devices were tested than are reported in Table 6. The impedances of the devices are representative of the range of impedances measured and have the most uniform after-plating impedances. Considerable care was taken with the equipment used to take the measurements to ensure the data were accurate. Unfortunately, the equipment used is inaccurate above of 20 MΩ so any entry 20+ MΩ implies that the impedance was greater than could be measured. Phase angles were from $72^{o}$ to $90^{o}$.

The plating rating refers to the appearance of the electrodes after they have been platinum plated. A good rating means that platinum is clearly visible on the electrode site and is black in color, denoting a convoluted surface. A poor rating means the surface did not plate or that the platinum formed a planar surface. It should be noted that 10 s of plating using 1 $\mu$A of current are sufficient to completely plate a 10 $\mu$m diameter electrode site.

The insulating layer on the devices tested is fairly thin, yet pinholing was not observed. Probes that underwent a slightly different insulation process displayed pinholing after the platinum plating. Because the tips are small, the entire tip ends up in the platinum plating solution. This results in platinum plating anywhere along the length of the tip that a pinhole occurs. Fortunately, this did not happen with the

Table 6

Electrode Impedance

Probe 3-5

Topside insulation -- 680 Å $Si_3N_4$ and 680 Å $SiO_2$
Substrate insulation-- 900 Å $Si_3N_4$ and 1700 Å $SiO_2$

| Electrode | Impedance Before Platinum Plating | Impedance After Platinum Plating | Plating Rating |
|---|---|---|---|
| 1 | $20^+$ MΩ | 250 kΩ | good |
| 2 | $20^+$ MΩ | $20^+$ MΩ | good |
| 3 | 250 kΩ | 67 kΩ | good |
| 4 | 125 kΩ | 67 kΩ | poor |
| 5 | $20^+$ MΩ | 77 kΩ | good |
| 6 | 200 kΩ | 143 kΩ | good |
| 7 | 200 kΩ | 143 kΩ | good |

Probe 3-6

Insulation - identical to probe 3-5

| | | | |
|---|---|---|---|
| 1 | $20^+$ MΩ | 143 kΩ | good |
| 2 | $20^+$ MΩ | 111 kΩ | good |
| 3 | $20^+$ MΩ | 125 kΩ | good |
| 4 | $20^+$ MΩ | 100 kΩ | good |
| 5 | 167 kΩ | 200 kΩ | good |
| 6 | $20^+$ MΩ | 111 kΩ | good |
| 7 | $20^+$ MΩ | 1.67 MΩ | good |

Probe 3-8

Insulation - identical to probe 3-5

| | | | |
|---|---|---|---|
| 1 | $20^+$ MΩ | 125 kΩ | good |
| 2 | $20^+$ MΩ | 111 kΩ | good |
| 3 | $20^+$ MΩ | 111 kΩ | good |
| 4 | 167 kΩ | 227 kΩ | poor |
| 5 | 1 MΩ | 167 kΩ | good |
| 6 | 83 kΩ | 111 kΩ | good |
| 7 | 100 kΩ | 111 kΩ | good |

devices reported and indicates that it is possible to deposit a thin uniform layer of insulation.

### 3.4.2. Shunt Impedance

The results of the shunt impedance measurements are recorded in Table 7. More devices were tested than are reported here, but these data are representative of all the devices. It should be noted that the insulation on these devices is thicker than that used on the working devices. This means that the shunt impedance of the working devices should be less than what is reported here. The impedance of these devices was tested using a 50 mV zero-to-peak signal to make certain the dielectric was not being broken down. The measurements were then done again, using a 1 V zero-to-peak signal in order to duplicate the test setup of the working devices. The change in voltage did not affect the impedance.

After testing, the devices were platinum plated in order to reveal any pinholes in the insulation. Probes 6 - 1 had one pinhole present on each of the conducting lines that terminate on electrodes 4 and 7. The other devices appeared pinhole free.

Table 7

Shunt Impedance

Topside insulation -- 800 Å $Si_3N_4$ and 1000 Å $SiO_2$

Substrate insulation-- 900 Å $Si_3N_4$ and 2600 Å $SiO_2$

| Probe 6-1 | | | Probe 6-2 | | |
|---|---|---|---|---|---|
| Electrode | Impedance | Phase | Electrode | Impedance | Phase |
| 1 | 20+ MΩ | 90° | 1 | 10 MΩ | 90° |
| 2 | 100 kΩ | 90° | 1 | 10 MΩ | 90° |
| 3 | 200 kΩ | 90° | 3 | 200 kΩ | 72° |
| 4 | 200 kΩ | 90° | 4 | 200 kΩ | 72° |
| 5 | 833 kΩ | 60° | 5 | 667 kΩ | 60° |
| 6 | 1 MΩ | 60° | 6 | 1 MΩ | 90° |
| 7 | 250 kΩ | 60° | 7 | 20+ MΩ | 90° |

# CHAPTER 4

# DISCUSSION

The results are both qualitative and quantitative. They need to be put together so that a process for fabricating a probe may emerge. In all cases the experiments were done in order to develop a process that would allow a region of the probe to be fabricated. The regions will be treated separately with enough overlap to allow integration of the regions into a single device.

## 4.1. Tip Formation

The results of the three experiments done with tip formation indicate that the process is very tolerant. Extrapolating from the results in Table 1 shows that an error of 1 or 2 hr in the diffusion process will only affect the tip thickness by 1 or 2 $\mu$m. Since this is a rather gross error in timekeeping, it is doubtful that there should be any problems in duplicating the results from one batch to another. The 10 hr predeposition followed by 1 hr drive is a short duration diffusion compared to the other two reported. Since it results in 10 $\mu$m thick tips, it is the process to be used.

Oxygen is vital during the predep. Without it the wafer surface becomes extremely pitted, preventing the patterning of the subsequently deposited tantalum. Another possible benefit of the oxygen is that the BN source wafers have never needed to be oxidized since the initial oxidation they were given at the beginning of the work. This is despite the fact that they have undergone more than 20 deep diffusions, of the type reported.

For all but a few of the diffusions oxygen was a fraction of the carrier gas. The oxidation that occurs during the diffusions is apparently enough to keep the wafers in working condition.

The tip etch is a critical step and either makes or breaks the probe. The results in Table 2 indicate that the slowly boiling EPW has the best combination of etch rate and probe quality. The probe quality is affected by precipitate formation and device usefulness after etching. For both parameters the slowly boiling EPW does the best job.

One point should be made about the etch rate reported for the PSE-100. The manufacturer claims an etch rate of 200 $\mu$m/hr or roughly five times what I found. This indicates that the amount of etchant used was insufficient for the amount of silicon placed into it. In light of this, the PSE-100 should greatly reduce the amount of time required to form a tip. However, its attack of tantalum still negates its use for these devices.

The experiment done to determine the etch rate of $P^+$ silicon in the EPW is inadequate to make any claims about the rate. It was originally thought that the frontside low doped silicon would etch at the same rate as the backside silicon. This does not appear to be the case when comparing the results for dice 1 - 3 with those for dice 4 - 6 (see Table 3). If it were the case, the change in the thickness of the $P^+$ region ($dP^+$) for dice 4 - 6 would be approximately one-half the change in the thickness of the P region (dP). This is a reasonable assumption since $dP^+$ for dice 1 - 3 is essentially 0, which indicates that the $P^+$ region does not etch. However, $dP^+$ for dice 4 - 6 does not equal 1/2 dP which prevents a reasonable calculation of an etch rate, since

the amount of data is insufficient. Reismann et al. [16] report an etch rate of 2 $\mu$m/hr for 0.001 $\Omega$/sq silicon. This is the approximate resistivity of a 7 x $10^{19}$ atoms/cc surface. Using this figure a 15 min error is allowable in the tip etch. An error of this length will result in losing approximately 1/2 $\mu$m in thickness of tip.

It is worth noting the effects of removing a probe before the etch is completed. With luck, a tip can be had that is approximately 50 $\mu$m thick for most of its length. The last 100 $\mu$m, or so, will be the desired 10 $\mu$m thick. This greatly enhances the strength of the tip without adding any process steps. Even though most of the tip is thick, the portion that actually pierces the animal's tissue is still thin enough to keep damage to a minimum.

## 4.2. Conductor Patterning

The goal of the conductor patterning experiments was to determine a repeatable method of patterning the tantalum. Two methods were discovered that do a very satisfactory job.

From Table 4 it is evident that only the first and last entries are suitable. For the other two it was impossible to prevent total photoresist dissolution before the tantalum was patterned. Both of the good methods result in an etch mask that is resistant enough to allow complete removal of excess tantalum. The method utilizing photoresist for a mask is superior simply because it eliminates the anodization step.

The results indicate that all etchants used etch tantalum very rapidly. This is good, as the solutions also attack silicon

and $SiO_2$ so the wafers should not be immersed for extended periods of time. One final comment about the etchant containing DI is that it should be mixed immediately prior to use. No quantitative results are available, but it was observed that etchant stored in a closed container for over a week required in excess of 20 min to etch the tantalum. This was never observed when using fresh etchant.

## 4.3. Insulation

More experiments were done with the insulation than with the other regions of the probe. This is an indication of how difficult it is to find a patternable dielectric that can survive the tip etch. The actual patterning of the insulation layer is not the difficulty. The problems arise when the probe is subjected to the tip etch.

### 4.3.1. Patterning

From Table 5 it is evident that methods exist for patterning the insulation layers. The best patterning method is the plasma etching of $Si_3N_4$. It is fast, patterns fine geometries, and does not use wet chemicals. Unfortunately, it affects the underlying tantalum which prevents its use for this work. This is a problem that can be remedied by using a different conductor that is not affected. The other method of patterning the $Si_3N_4$ is satisfactory but requires a lot of time. Ghandi [11] reports that higher concentrations of $H_3PO_4$ will etch faster and it is recommended that these be used in the future. Although not evident from the results, it is important to determine the complete removal of $Si_3N_4$ from a tantalum layer using

microprobes. By determining the conductivity of the surface, one can decide when to stop etching. This is particularly useful when only small areas of tantalum will be exposed.

The lift-off technique used with the SiO is a reasonable way to pattern that material. A couple of suggestions are in order to aid in the process. The first is that the photoresist should be blanket exposed after development. The other is that a heat sink should be used during deposition to prevent extreme baking of the resist. Both aid in removing the photoresist after the SiO is deposited.

The process of patterning the $Ta_2O_5$ is incorporated into the growth of the pentoxide, which makes it the easiest insulation layer to use. Another advantage of the $Ta_2O_5$ is that it adheres extremely well to the tantalum and has never been observed to peel. Unfortunately, large voltages are required to grow thick layers, and the tantalum is consumed in the process. It is reasonable to grow a 1000 Å layer for use as an initial insulation layer. This would reduce the amount of deposited insulation required and would guarantee passivation of the tantalum.

### 4.3.2. Sequencing Deposited Layers

The experiment to determine the sequence to deposit the layers was not exhaustive. Only three wafers were used, and it is difficult to claim repeatability from such a limited sample. One problem that has occurred with the five-layer structure is warping of the wafer. This is not surprising considering nearly a micron of material was deposited on the wafers. While this

makes it difficult to do subsequent patterning, it is not an insurmountable problem. One solution is to deposit films on the front and backsides of the wafer to balance the stress. Another is to deposit thinner layers, which addresses another problem that has occurred. The layers peel off the wafers spontaneously. Several wafers that had the sequence of layers deposited as reported earlier had severe cracking and peeling. Presently, work is being done on similar probes that have one-fourth the thickness of insulating layers. No cracking or peeling has occurred on these wafers, which indicates that the insulation layer needs to be thin to prevent peeling.

The $SiO_2$ on $Si_3N_4$ insulation offers the best insulating layer. It is readily deposited, easy to pattern, and resists the tip etch. It also adheres to the wafer if the layer is thin enough. So far, no problems have occurred with it and the tantalum.

### 4.4. Electrode Impedance

The results of the electrode impedance measurements are broken down according to working devices and devices used to measure shunt impedance. Each will be discussed separately and then compared to make suggestions about future work.

#### 4.4.1. Series Impedance

The most notable result contained in Table 6 is the uniformity of the electrode impedances after platinum plating. Many of the values lie between 100 kΩ and 200 kΩ. Actual recordings of cockroach nerve signals have not been made with these devices, so it is difficult to say if this value is small

enough to give a reasonable signal-to-noise ratio. However, because the impedances are so close to one another in value, it is reasonable that each channel will have approximately the same SNR. This means that all channels will be useful for recording, because they can detect the same minimum amplitude signal. If a channel has a low SNR then small amplitude signals will be drowned out on it while being present on a channel with a large SNR. The perceived spatial distribution of the signal would be distorted if this occurred.

An interesting result is the increase in impedance of some of the electrodes after platinum plating. Electrode 5 of probe 3-6 is one example. Even though this electrode is obviously plated, its impedance has increased. I offer no explanation of this and assume it is an anomaly.

The lack of pinholes in this thin insulation layer is further testimony to the usefulness of CVD insulating layers. The probes tested underwent the tip etch so the insulation layer has survived all the processes required to make a probe. Work remains to determine how long a device may reside inside an animal before the insulation deteriorates.

### 4.4.2. Shunt Impedance

Many of the shunt impedance values are of the same order of magnitude as the electrode impedances, which are much less than the theoretical shunt impedance. Using a 100 $\mu$m length of 5 $\mu$m wide line and the insulation thicknesses reported, a shunt impedance of 91 M$\Omega$ is calculated for a 1 kHz signal. This suggests that the insulating layers are too thin, because much of

the signal appearing across the probe will be passed to ground. The shunt impedance should be much greater than the electrode's series impedance. The problem is compounded when the data in Table 6 are compared with the data in Table 7 because the insulation on the devices reported in Table 7 is 40% thicker than that on the devices reported in Table 6. A reasonable approximation is that the shunt impedance is linear with insulation thickness. Reducing all the shunt impedances by 40% puts them very nearly equal to the electrode impedance, which is a parallel combination of shunt and series impedances. This indicates that the series is larger than the shunt impedance. However, for an accurate analysis, the shunt impedance should be measured for each group of probes.

The phase angles recorded for the shunt impedance measurements indicate a large amount of pure resistance in the circuit. A typical sheet resistance for the tantalum films used is 13Ω/sq, which yields a conducting line resistance of approximately 5000Ω. This value is nearly two orders of magnitude less than the shunt impedances recorded, so it cannot account for the shift in phase away from $90^{o}$.

A reasonable explanation for the shift in phase away from $90^{o}$ is that the insulation layer contained pinholes, that were not detected by platinum plating. Two results from the electrode impedance measurements lend support to this theory. The first is that the platinum plating process does not always result in a visible coating of platinum on the tantalum. Since this process was used to detect pinholes it is possible that pinholes were present that did not plate and were not detected. Second, the

electrode impedances measured contain phase angles from $72^{o}$ to $90^{o}$, so it is possible for the metal-saline interface not to appear totally capacitive. Pinholes would provide a metal-saline interface which could then account for the phase angles recorded.

4.4.3. Impedance

Improvement in the electrode impedance will come about by increasing the thickness of the insulating layers. The probe has two ground planes that the tantalum must be insulated from. The saline solution is the first, and the top side insulation isolates the tantalum from it. The heavily doped silicon substrate has a very low resistance and serves as the other ground plane. The substrate insulation isolates the tantalum from the silicon. There are several possible ways to increase the insulation layers which are outlined below.

4.4.3.1. Topside Insulation

The topside insulation can be increased by depositing a thicker layer on the device or by growing $Ta_2O_5$ on the tantalum. Depositing a layer is the most convenient, but is limited in thickness due to the built-in tensile stress on the layer. The high temperature CVD reactor appears to be limited to about 5000 Å of material before peeling and cracking of the film occurs. Low temperature reactors are available, and future work should use these in order to increase the thickness of the insulation. Films deposited at low temperatures have less built-in stress than those deposited at high temperatures so it should be possible to deposit a thicker layer.

Growing a layer of $Ta_2O_5$ on the tantalum avoids the problem

of the insulation peeling. However th,e conductor is consumed during growth, and oxide thicknesses are limited by the forming voltage. A 2000 Å thick layer requires a 120 volt forming voltage. The best solution is probably a combination of the two techniques. The grown oxide will ensure passivation of the metal, and the deposited layer will provide the necessary thickness to increase the shunt impedance.

4.4.3.2. Substrate Insulation

The easiest way to increase the substrate insulation thickness is to grow a thicker oxide on the silicon. One possible problem with this is a change in the diffusion profile which could result in a different tip thickness. This should be easily accounted for after several trials. The other method for increasing the substrate insulation thickness is to deposit more materials. The difficulties and possible ways of doing this have already been discussed.

# CHAPTER 5

# CONCLUSION

A device has been made that holds promise for making multichannel recordings of an animal's nervous activity. Actual recordings have not been made due to restrictions on time. The device combines extremely fine geometries with the ability to be mass produced. Several processes are worth summarizing, since they have the potential to be used in novel ways.

## 5.1. Silicon Machining

The 10 hr 1175$^{o}$C boron predeposition followed by etching the EPW has been used repeatedly for nearly one year, with the exact same results every time. It should be possible to use this technique to form a multitude of fine, precisely controlled structures in silicon. Indeed, the automobile industry uses a similar process in the manufacture of thousands of miniature pressure sensors every day. This is adequate testimony for the reliability of the process.

## 5.2. Conducting Layer

Tantalum is a very good choice of conductor when a refractory material is needed. It will survive high temperatures, is easily patterned using photoresist for an etch mask, and has an insulating native oxide. The oxide gives another degree of freedom to the problem of insulating the metal as it is easily grown and patterned. Finally, bonding to tantalum can be easily done using aluminum wire and an ultrasonic bonder. Its future use is strongly recommended, as it has not

exhibited any bad points during the course of this work.

## 5.3. Insulating Layer

High temperature CVD can be used to create a probe which has a uniform, pinhole free, insulating layer. To improve the shunt impedance, a thicker layer should be deposited; however, peeling occurs when the layer is too thick. This suggests that future work should address the problem of applying a thicker layer of insulation. Several possible ways of doing this are outlined in Section 4.4.3.

## 5.4. Final Word

The processes given in this thesis allow a probe type microelectrode to be built. The use of microelectronic processing techniques results in a device whose dimensions are precisely controlled, which will aid in evaluating the spatial distribution of a nerve signal in a nerve. The choice of substrate material allows the future integration of electronics, which will greatly enhance the capabilities of the device. Finally, the ability to produce many identical devices gives the researcher the confidence that observed variations in nerve signals are just that and not differences in device parameters.

# REFERENCES

[1] K. D. Wise and K. Najafi, "A micromachined integrated sensor with on-chip self-test capability," IEEE Solid-State Sensor Conf., 1984.

[2] J. Kruger, "A 12-fold microelectrode for recording from vertically aligned cortical neurones," J. Neuroscience Methods, 6, 347, 1982.

[3] J. Kruger and M. Bach, "Simultaneous recording with 30 microelectrodes in monkey visual cortex," Exp. Brain Res., 41, 191, 1981.

[4] R. S. Pickard, "A review of printed circuit microelectrodes and their production," J. Neuroscience Methods, 1, 301, 1979.

[5] G. A. May, S. A. Shamma, and R. L. White, "A tantalum-on-sapphire microelectrode array," IEEE Trans. Electron Devices, ED-26, 1932, 1979.

[6] M. Kuperstein and D. A. Whittington, "A practical 24-channel microelectrode for neural recording in vivo, IEEE Trans. Biomed. Eng., BME-28, 288, 1981.

[7] K. D. Wise, J. B. Angell, and A. Starr, "An integrated circuit approach to extracellular microelectrodes," IEEE Trans. Biomed. Eng., BME-17, 238, 1970.

[8] A. Bohg, "Ethylene diamine-pyrocatechol-water mixture shows etching anomaly in boron-doped silicon," J. Electrochem. Soc., 118, 401, 1971.

[9] M. M. Picus, "Fabrication of a nine channel probe-type microelectrode array," Thesis (M.S.), University of Illinois at Urbana-Champaign, 1983.

[10] L. I. Maissel and R. Glang, eds., Handbook of Thin Film Technology, McGraw-Hill, NY, 1970.

[11] S. K. Ghandi, VLSI Fabrication Principles, Wiley, NY, 1983.

[12] J. Pine, "Recording action potentials from cultured neurons with extracellular microcircuit electrodes," J. Neuroscience Methods, 2, 19, 1980.

[13] R. B. Fair, "Boron diffusion in silicon-concentration and orientation dependence, background effects, and profile estimation," J. Electrochem. Soc., 122, 800, 1975.

[14] A. M-R. Lin, D. A. Antoniadis, and R. W. Dutton, "The oxidation rate dependence of oxidation-enhanced diffusion of boron and phosphorous in silicon," J. Electrochem. Soc., 128, 1131, 1981.

[15] J. S. Hughes, "Ultrasonic wire bonding to thin films," Thesis (M.S.) University of Illinois at Urbana-Champaign, 1980.

[16] A. Reisman, M. Berkenblit, S. A. Chan, F. B. Kaufman, and D. C. Green, "The controlled etching of silicon in catalyzed ethylenediamine-pyrocatechol-water solutions," J. Electrochem. Soc. 126, 1406, 1979.