A DATA ACQUISITION SYSTEM FOR ULTRASONIC TOMOGRAPHY

BY

KENNETH CHAN

B.S., University of Illinois, 1977

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 1980

Urbana, Illinois

Acknowledgements

The author wishes to express his grateful appreciation to advisors Professor William D. O'Brien, Jr. and Raymond Fish, M.D., Ph.D., for suggesting this thesis topic, and for their encouragement and guidance throughout this investigation. Special thanks are also extended to Dr. Ronald Johnston for his help and suggestions in testing the Data Acquisition System, Mr. Shaw Moldauer for developing the system power supply and major construction works of the system, Mr. Tom Nall for constructing the system front panel, Mr. Bruce McCormick for testing the programmable gain amplifier and laying out of printed circuit boards, Mr. Bob Amirian for constructing the buffer amplifier and cables and plotting of frequency response curves, Mr. Bob Cicone for his drafting assistance, Mr. Sam Law for initial plotting of frequency response curves by computer and Mrs. Wanda Elliott for typing this thesis. Finally the author wishes to thank his parents, for their support and encouragement through his education and his wife, Rosanna, for typing drafts I and II of this thesis, and for her constant patience, support, and encouragement through this difficult period.

Table of Contents

Chapter		Page
1	Introduction.	1
2	Overall System Concept.	3
3	Interface With Perkin Elmer 7/32 Minicomputer	10
4	System Components	15
5	System Evaluation	100
6	Recommendations for System Improvement.	106
List of References		109
Appendix A - Schematics.		110
Appendix B - Suggested Vendors of Integrated Circuits.		161
Appendix C - List of Symbols		163

Chapter 1

Introduction

Computer-assisted tomography (CAT) is a well established diagnostic imaging technique used in hospitals and X-ray is used instead of ultrasound. A conventional X-ray system takes pictures by passing X-rays through the body and detecting them with a photographic emulsion. The different tissues in the body attenuate the X-ray beam differently, and the film responds to the intensity of the X-rays falling on it. The resulting image displays the accumulated attenuation of the original beam. This conventional X-ray imaging scheme has the disadvantage of losing depth information, but more importantly is the confusion of overlapping planes which makes detection of subtle abnormalities difficult or impossible. Details in soft tissue simply cannot be discerned on a conventional X-ray picture. CAT however restricts the thickness or height of the X-ray beam to about 1 cm or less and scans a line in a single view. Many of these views are taken at different angles. The resulting reconstructed CAT picutre is a cross section of the patient. These tomographic images have the advantage of offering an uncontaminated display of the layer of the patient's body under examination and subtle differences in soft tissue density are clearly delineated.

This thesis describes a data acquisition system used in an ultrasonic computer-assisted tomography system. This data acquisition system measures the frequency dependent amplitude and time-of-flight of ultrasound after it passes through biological materials. This information is processed to produce tomographic images of the material being studied. In this discussion, Chapter 1 gives the reader a general introduction. Chapter 2 shows the overall system concept with reference to the system block diagram. Chapter 3 discusses the interface

philosophy with the Perkin Elmer 7/32 minicomputer. Chapter 4 describes the different data acquisition electronics and the power system. Chapter 5 evaluates the whole system by stating the results of time-of-flight and absorption measurements. Chapter 6 discusses the recommendations for system improvement. Schematics of circuits are given in Appendix A and Appendix B gives the suggested vendors of integrated circuits. Appendix C gives a list of symbols together with their definitions.

Chapter 2

Overall System Concept

2.1 System Description

The system block diagram is shown in Figure 2-1. The image reconstruction tasks and experiment controls are handled by a Perkin Elmer 7/32 minicomputer and communications of the data acquisition system to the Perkin Elmer 7/32 are performed by an analog-to-digital (A/D) input channel and two digital input/output ports (DIO). A system controller is responsible for interfacing the different system data acquisition electronics to the Perkin Elmer 7/32 computer.

The transmitted ultrasound signal ranges from a broadband pulse to a discrete frequency tone burst. The signal source is an HP 8660B sine wave synthesizer (output frequency range = 0.01 - 110 MHz) whose frequency and amplitude are programmable and controlled by the 7/32 computer. The synthesizer drives a programmable window generator and a selectable delay line. The programmable window generator utilizes high speed Schottky TTL logic chips which have minimal gate delays to produce a window coherent with the signal zero crossings. This window has a capability of producing a window whose width is equivalent to 0.5, 1, 2, 4, 8, 16, 32, 64, or 128 cycles of the signal. The selectable delay line (32 ns or 42 ns delay) delays the synthesizer signal such that the zero crossing of the synthesizer signal matches with the zero crossing of the window. The 30 ns delay is selected when a broadband pulse (0.5 cycle) is transmitted and the 42 ns delay is selected when a discrete frequency tone burst is transmitted. The window signal and the delayed systhesizer signal are mixed by the double balanced mixer (DBM) and a pulse of appropriate pulse width is thus produced. The

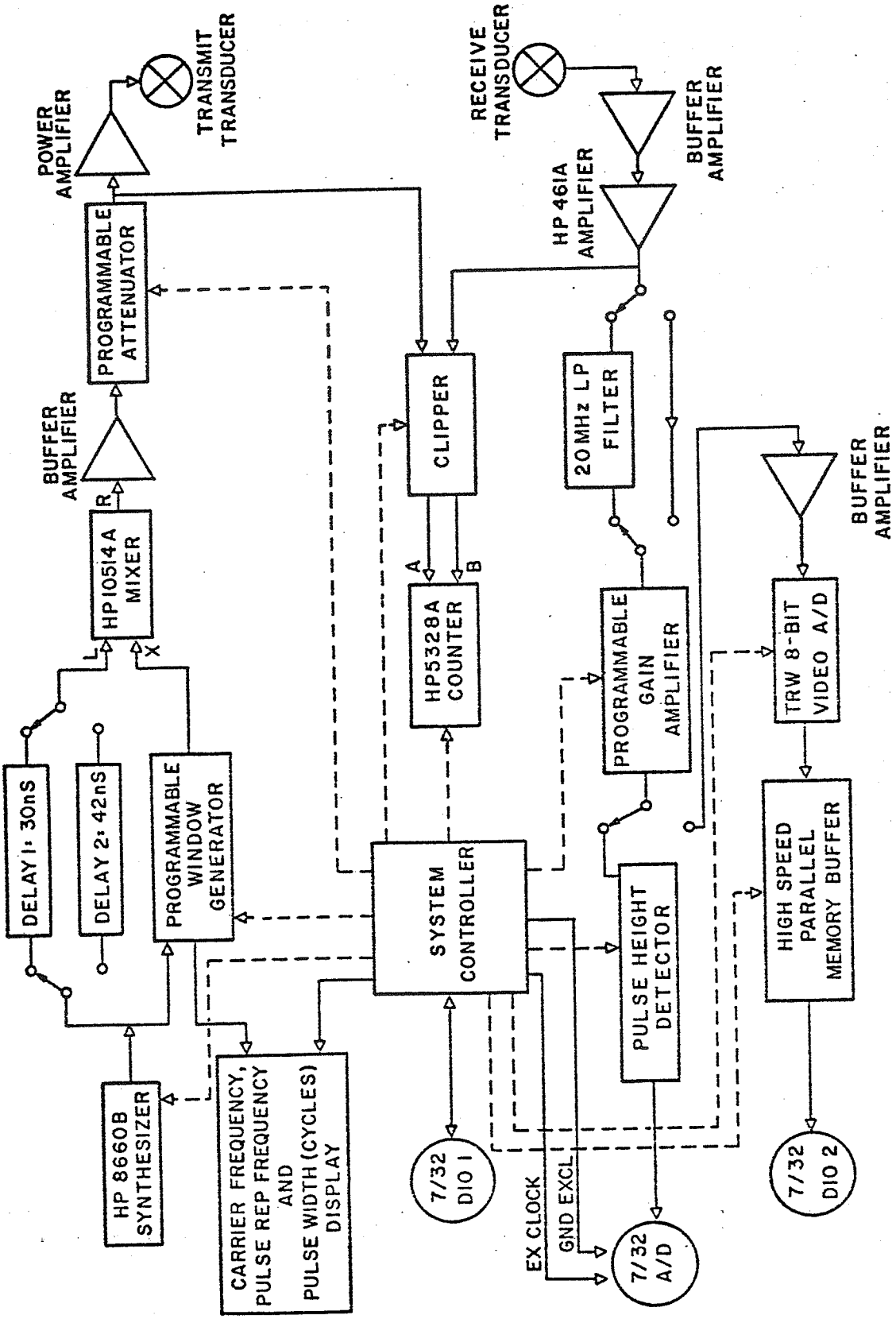


Figure 2-1: System Block Diagram

DBM output drives a buffer amplifier which then drives a programmable attenuator. The programmable attenuator varies the signal output of the DBM in factors of two and provides a dynamic range of 36 dB to the transmitter channel. The attenuated signal at the output of the programmable attenautor is then amplified by a power amplifier which in turn excites the transmit transducer and transmits an ultrasound signal through the tissue under test.

An HP 5328A universal counter is used for the time-of-flight (TOF) measurements of the ultrasound signal. A 10 ns resolution is achieved with single shot TOF measurements and a 2 ns resolution is achieved by averaging 100 intervals. The HP 5328A universal counter is started by triggering its channel A input by a falling edge generated by the clipper. The clipper is a signal detection circuit which generates a falling edge to trigger channel A of the counter when any signal occurs at the programmable attenuator output.

After the signal passes through the tissue under test, it is detected by an ultrasonic transducer. The transducer output drives a buffer amplifier which in turn drives the HP 461A amplifier which amplifies the received ultrasound signal. The amplified signal causes the clipper circuit to generate another falling edge to trigger channel B of the HP 5328A counter and thus stopping the counter after the appropriate number of intervals, thus yielding time-of-flight data. When discrete frequency tone bursts are transmitted, the HP 461A drives a 20 MHz low pass filter to reduce noise. The filtered signal is then further amplified by a programmable gain amplifier to condition the signal to an appropriate amplitude range of the pulse height detector (PHD). The pulse height detector produces a DC level output proportional to the peak, rectified signal amplitude. This DC level is then digitized by an analog-to-digital (A/D) converter in the Perkin Elmer 7/32 through an A/D input channel. This receiver channel has an overall dynamic range of 105 dB.

The filter and the pulse height detector are by-passed for a broadband pulse. The signal output of the HP 461A is amplified by the programmable amplifier and goes through a buffer amplifier to an 8-BIT video analog-to-digital converter (TRW's TDC 100 TJ) which has a sampling rate of 30 MHz. A high speed parallel memory buffer must be used to buffer all the data points. A parallel memory system is used to obtain a high data transfer rate. Thus by sequential clocking of several blocks of slower memories, a higher bandwidth is achieved to match the 30 MHz sampling rate. This memory buffer empties its contents into the Perkin Elmer 7/32 through DIO 2. Appropriate signal processing such as Fourier analysis can then be performed.

The above described system is contained in three chassis termed the system controller, the data acquisition system (contains all the data acquisition electronics), and the power supply.

It is to the attention of the reader that the TRW 8-BIT video analog-to-digital converter and the parallel memory buffer are not implemented in the present system and their designs will not be discussed in this documentation. See Foster (1) for details.

2.2 System Front Panel Description

The system front panel refers to the front panel of the Data Acquisition System chassis. Figure 2-2 shows the system front panel. The reader should also refer to Figure 2-1 in the following discussions.

The seven segment displays on the upper left corner of the front panel gives information of the carrier frequency (output signal frequency of the HP 8660B synthesizer), the pulse repitition frequency of the tone burst and the pulse width (or no. of cycles) of the tone burst. The ultrasound tone burst generation

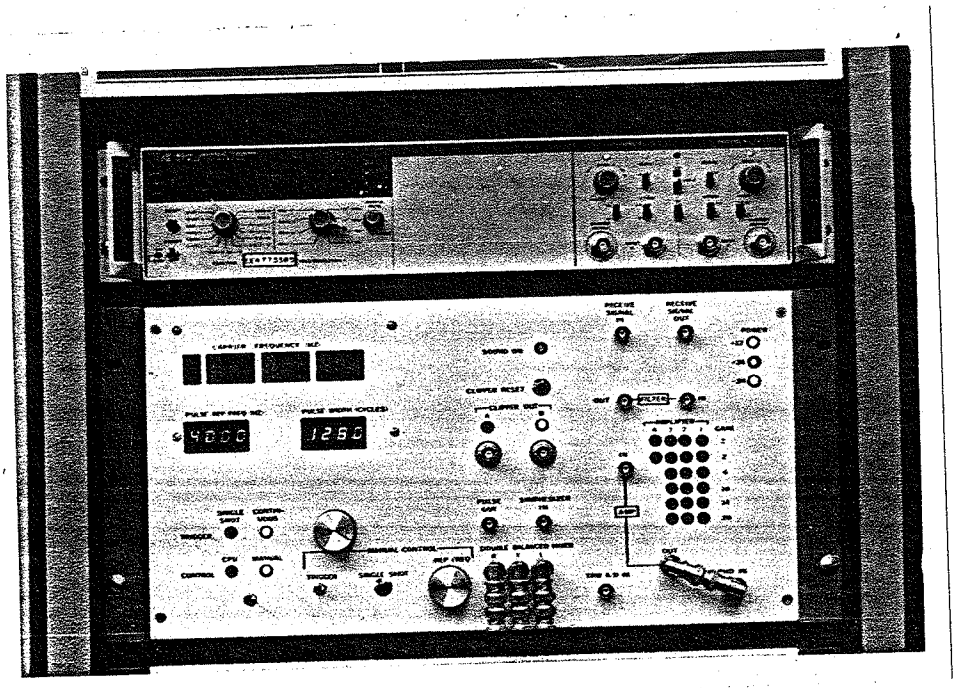


Figure 2-2: System Front Panel

can be continuous triggered or single shot triggered. The lighted LED in the corresponding position will show the type of trigger used. The pulse repetition frequency display gives the continuous trigger frequency. Triggering can be either CPU (i.e., the Perkin Elmer 7/32) or manually controlled and this is selected by the toggle switch under the control mode LED's. The lighted LED in the corresponding position will show the trigger control source. During the manual control mode, the three switches under the manual control section controlls the triggering. The type of trigger is selected by the TRIGGER toggle switch. A press on the SINGLE SHOT push button will cause a single transmission of the ultrasound signal. The REP FREQ knob selects the pulse repetition frequency. The pulse width or number of cycles of the ultrasound signal is always manually selected by the knob under the PULSE WIDTH (CYCLES) display.

The SOUND ON (yellow) LED gives indication of ultrasound generation during the CPU control mode. The LED will stay on during the continuous trigger mode and will give a blink on every single shot trigger. The CLIPPER RESET push button allows the user to manually reset the clipper. The clipper is reset when the clipper channel A output LED is on (corresponding to a TTL "high") and when the channel B output LED is off (corresponding to a TTL "low"). The two BNC jack under the output LED's gives the output of the clipper circuit. The HP 8660B synthesizer signal output goes to the SYNTHESIZER IN BNC jack. The PULSE OUT BNC gives the output of the programmable attenuator and this signal should be routed to the input of the power amplifier as seen on Figure 2-1. The programmable attenuator output is connected to the clipper input inside the chassis. The double balanced mixer's R, X, and L terminals go to the R, X, and L BNC's under double balanced mixer. The L terminal accepts the delayed synthesizer signal and the X terminal accepts the window. The R output terminal of the mixer

is connected to the buffer amplifier input.

The HP 461A amplifier output goes to the RECEIVE SIGNAL IN BNC. This signal is routed to the second clipper input and rerouted out to the front panel as the RECEIVE SIGNAL OUT. When a discrete frequency tone burst is transmitted, RECEIVE SIGNAL OUT is connected to the IN BNC of the filter (20 MHz low-pass) and the OUT BNC of the filter is connected to the IN BNC of the AMP--the programmable gain amplifier. The OUT BNC of AMP is then connected to the PHD IN BNC, which is the input to the pulse height detector circuit. The pulse height detector output is available at a BNC (PHD OUT) at the back of this chassis. When a broadband pulse is transmitted, RECEIVED SIGNAL OUT is connected directly to the IN BNC of AMP and the filter is by passed. The OUT BNC of AMP is then connected to the TRW A/D IN BNC which is the input to the buffer amplifier before the TRW 8-BIT video A/D. Since this buffer amplifier, the TRW 8-BIT video A/D and the high speed parallel memory buffer are not implemented in the present system, the TRW A/D IN BNC has no function at all. The LED amplifier gain table is not implemented as it was originally designed for use with an earlier design of the programmable gain amplifier. The three LED's under POWER indicates the functioning of the system power supply.

Chapter 3

Interface With Perkin Elmer 7/32 Minicomputer

3.1 Introduction

The system interfaces with the 7/32 through two digital input/output ports (DIO 1 and DIO 2, Perkin Elmer Part no. M48-450) and an analog-to-digital (A/D) input channel. The DIO's have 16 bit (TTL level) output, 16 bit (TTL level) input, and four hand-shake signals (OPDR, OPDA, IPDR, and IDA).

DIO 1 is mainly for communications between the 7/32 and the system controller. The system controller is a collection of device controllers controlling the different system devices. DIO 2 is responsible for removing data from the local high speed parallel memory buffer. The A/D input channel accepts the DC output of the pulse height detector. This DC level is then digitized by the built-in A/D of the 7/32. The A/D has a 0.2% accuracy, 0 V to - 10.24 V dynamic range, 10-BIT resolution and 12 kHz sampling rate.

3.2 Interfacing with DIO 1-- the System Controller

Due to the limited digital input/output facilities of the 7/32 (i.e., only two DIO's), an external processor bus is implemented to control and communicate with the different system devices. A block diagram of the system controller is given in Figure 3-1 in which DIO I is communicating with the different system devices through the individual device controllers. The system controller has a capability of controlling sixteen different devices. As mentioned earlier, there are four hand-shake signals and only OPDA (output-data-available) is used in this external processor bus configuration. The OPDA, which is a 2 μs pulse (TTL

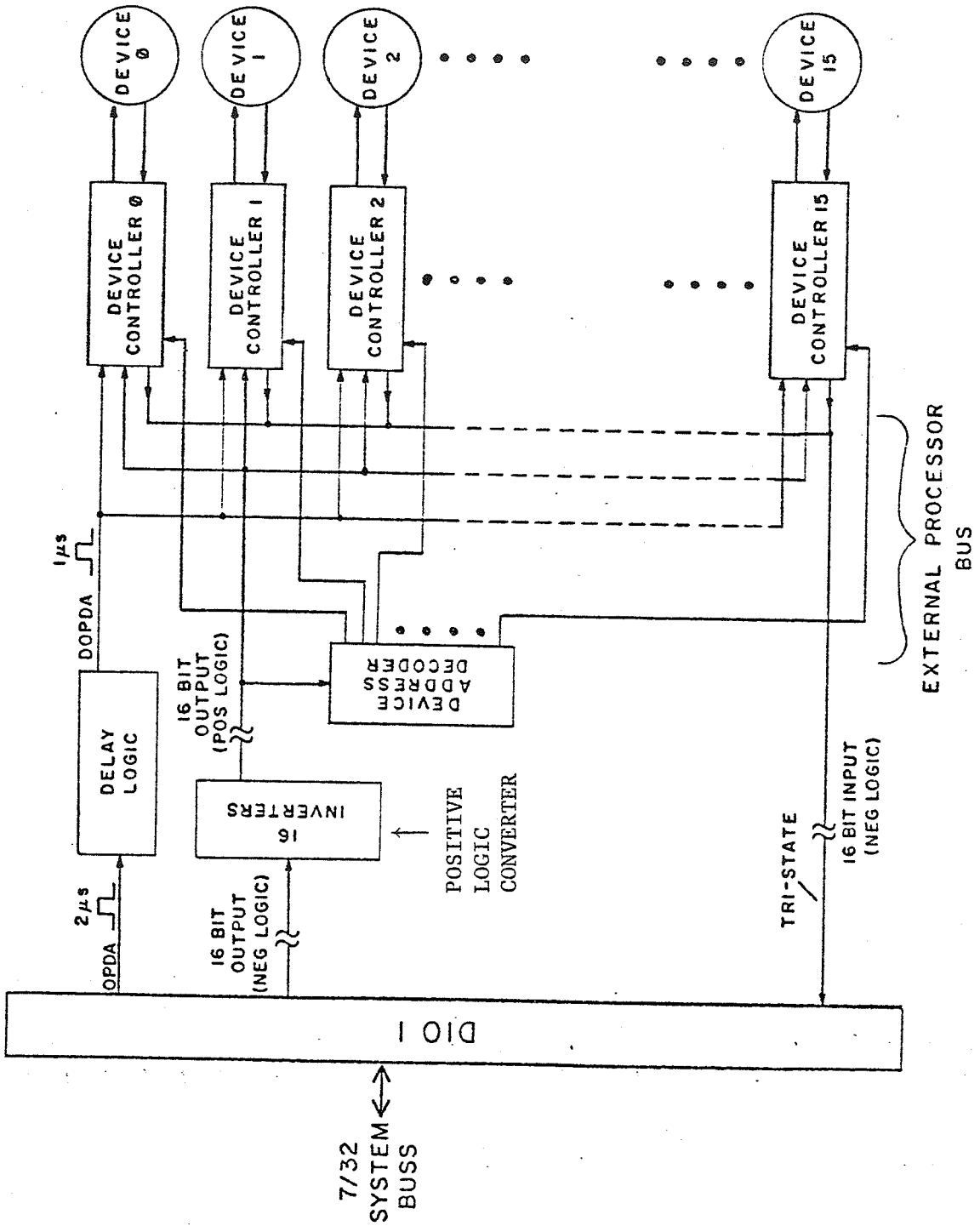
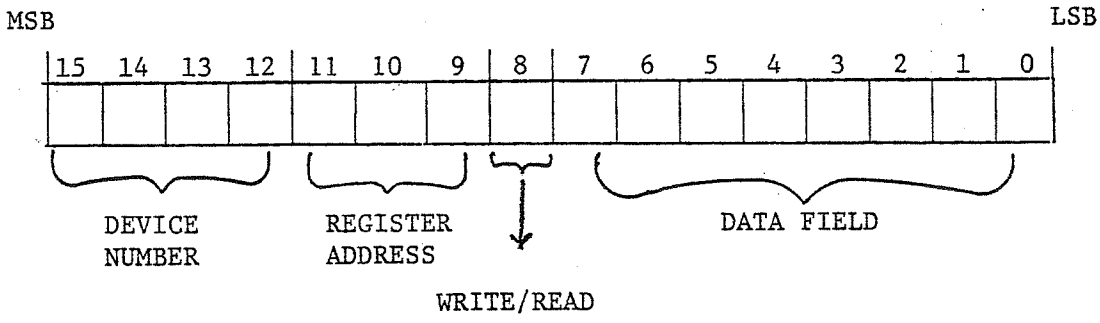


Figure 3-1: The System Controller

level), is asserted by the 7/32 when a Write Halfword (WH) instruction is executed to provide data at the 16 bit output to the device controllers.

Every device controller has an address and eight 8-BIT addressable registers. These registers can be divided into two types according to their function, i.e., control status registers (CSR) and buffer registers (BUF). The CSR's are responsible for storing the control bits of the device and the BUF's are responsible for storing the data bits required for programming the device. The bits of the CSR's and BUF's can be write-only, read-only, or read/write bits. A general control word format for a device controller is given in Figure 3-2. Hence to program a device, the user must write into the 16 bit output specifying the device number, the register address, whether write or read, and the data. Only devices 0 to 6 are implemented in this data acquisition system. To write into any register in any device controller thus requires a Write Halfword instruction. To read the registers, however requires first writing into the 16 bit output specifying the device number, register address and read mode, and then a Read Halfword (RH) instruction will read the register into the 16 bit input. During



* In all fields of the control word, the MSB is always left justified.

Figure 3-2: General Control Word Format

the read mode, the Write Halfword instruction is required to enable the tri-state drivers of the particular controller to drive the 16 bit input. It must be noted that although the registers are 8 bits long, a read-only register can be 16 bits long. Sixteen bit read-only buffer registers are implemented in the device controller of the HP 5328A Universal Counter. A delayed OPDA (DOPDA) is generated by using the falling edge of OPDA to trigger a 1 μs one-shot for strobing the 16-bit output into the device controllers. This is essential because time must be allowed for the output bits to settle. It is noted that the 16 bit input and output of DIO I is in negative logic.

Sixteen inverters are used to convert the 16 bit output into positive logic. This makes it easier in the design of the device controllers because the address decoders in the system controller accepts positive logic. The inverter logic and the OPDA delay logic are on Board D2 (Figure A-1 of Appendix A). On Board D2, IC's (BY), (CY), and (DY) are the inverters for inverting the 16 bit output from the 7/32 to positive logic. IC (CZ) is generating the 1 μs one-shot (DOPDA) upon seeing the falling edge of OPDA.

While the 7/32 configuration has OBIT 15 (output bit 15) as the least significant bit at the 16 bit output and IBIT 15 (input bit 15) as the least significant bit at the 16 bit input, the bit numbering system is reversed in the configuration of this data acquisition system, i.e., OBIT 15 is renamed as OBIT 0 and IBIT 15 is renamed as IBIT 0. The 16 bit output from DIO 1 of the 7/32 is routed to Board D2 through connectors BB4 and BB0 and the 16 bit input through connectors BB5 and BB1. The 16 bit outputs and 16 bit inputs are rerouted out to the back panel of the data acquisition system to allow other users of the 7/32 to access to DIO 1. The 16 bit outputs are rerouted through connectors BB2 and

LL1 and the 16 bit inputs are rerouted through connectors BB3 and LL2. A detail discussion on the design and circuit of the different device controllers is given in Chapter 4, System Components, together with the device they control.

3.3 Interfacing with DIO 2

DIO 2 is mainly used to read the data points stored in the high speed parallel memory buffer during the broadband pulse mode. The broadband pulse section with the high speed parallel memory buffer, the TRW 8-BIT video A/D and the buffer amplifier before the A/D is not implemented in the present system. The reader is referred to Foster (1) for details.

3.4 Interfacing with A/D Input Channel

The A/D (analog-to-digital) input channel accepts the DC output of the pulse height detector and digitizes this DC voltage with the 7/32 A/D converter (Perkin Elmer part no. M48-214). The interface signals are EX CLOCK and GND EXCL. EX CLOCK is a 750 ns clock pulse triggered by the falling edge of the Clipper's B output. This clock pulse tells the A/D converter of the 7/32 to start digitizing the pulse height detector output. Since EX CLOCK is asserted upon seeing the falling edge of the Clipper's B output, the user should program the A/D converter of the 7/32 to continuously sample the pulse height detector output and pick the maximum value as the valid pulse height detector output.

GND EXCL is a bit in the control word of the pulse height detector controller. This bit must be set to logical 0 in order for the A/D converter of the 7/32 to work with EX CLOCK.

Chapter 4

System Components

4.1 Signal Generation and Data Acquisition Devices

4.1.1 HP 8660B Synthesizer

4.1.1.1 Device Description

This is the signal source of the data acquisition system. The HP 8660B synthesizer has an output (sine wave) range of 0.01 - 110 MHz. The continuous wave (CW) frequency and output level are remotely programmed by the 7/32 DIO 1 through the device controller of this device. The CW frequency is programmable in 1 Hz steps over the full frequency range of the HP 86601A RF section plug-in and the amplitude of the RF output signal is programmable in 1 dB steps over the output range of the RF section (i.e., 1 V_{rms} to 0.01 μV_{rms}). Programming of the RF output is done by setting the attenuator at the output section of the HP 86601A RF section in dBV. See reference(2) for programming examples. The synthesizer is programmed to give a fixed 1 V (zero to peak) output and only the CW frequency is varied during its utilization. The T network on the zero-crossing detector board, which serves to route the synthesizer signal to the delay lines, attenuates the synthesizer signal to 0.5 V (zero to peak) should the snythesizer be programmed to give a maximum 1 V_{rms} output. This 0.5 V (zero to peak) maximum limit is essential in order not to exceed the maximum input power requirement of the double bananced mixer. It was however observed that the synthesizer signal should not exceed 1 V (zero to peak) for good tone-burst signal generations and higher signal levels would cause the peaks of the sine wave cycles of the tone-burst to be clipped. There is also a frequency stepping mode in which a desired frequency step size may be programmed into the internal memory in the

8660B mainfrane and simple programming commands will then increment the output frequency up or down by the selected step size. Minimum step size is 1 Hz and maximum step is limited only by the frequency range of the HP 86601A RF section. This mode however is not encouraged due to the impossibility of displaying the new signal frequency on the system front panel after stepping.

4.1.1.2 Programming Format

The HP 8660B is programmed in negative true logic, i.e., any level between 0 V and +0.4 V will be read as logic "1" and levels between +2.4 V and +5 V will be read as logic "0." A logic "1" at pin 5 of the remote inputs connector on the rear panel of the HP 8660B will switch the instrument into remot operation and disable all front panel controls except the power line ON/STANDBY switch. A front panel light indicates remote operation.

Programming is accomplished by eight data lines and one command line in a BCD serial code. The procedure is as follows:

1. Numerical data is entered into an internal "temporary" register two digits at a time, beginning with the least significant digits. The pairs of digits are entered on two sets of four lines in 1-2-4-8 BCD code. When the eight bits of data are on the lines, the loading is initiated by the negative-going portion of a command pulse entered on a separate command line. Entry of each two digits take 1.25 μs, and during this period a "busy" (FLAG) line is grounded. This sequence is repeated for each two digits until all have been entered.
2. When all ten numbers are entered, "15" is entered on one set of four lines (all four lines held low and corresponding to digit 1 of the eight data lines) and the address of the function to be controlled is

entered on the other four lines (digit 2). Another command pulse entered on the command line then initiates execution of the programmed function.

3. A positive-going signal on the "busy" (FLAG) line indicates that switching has been completed and the instrument is ready for a new measurement. Examples of programming this instrument are given in reference (2). Programming of the various functions of the instrument may be done in any order. However, when more than one function is to be changed between measurements it is usually advantageous to program the slower function first to minimize set-up time. Programming times for the various functions are discussed in reference (3).

4.1.1.3 Internal Data Register System

The internal data register system of the HP 8660B is shown in Figure 4-1. All data is first entered into a ten digit temporary storage register two digits at a time. From there the data is routed to one of five functional registers.

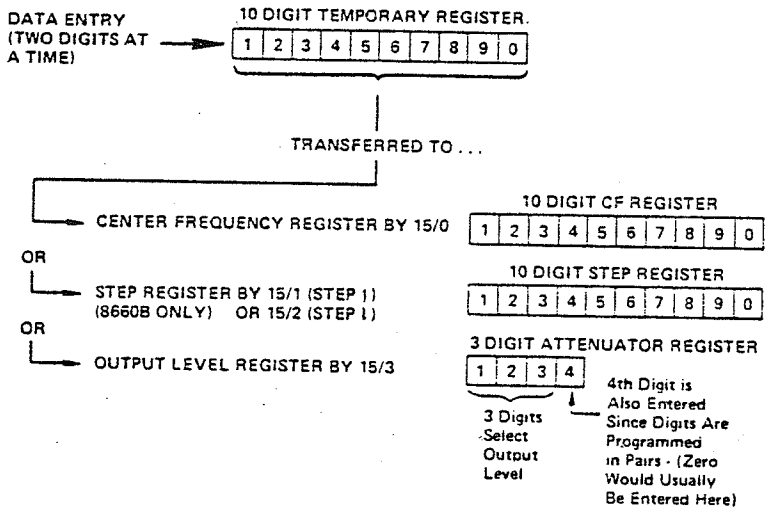


Figure 4-1. HP 8660B Internal Data Register System

The particular register the data is transferred to is determined by the qualifier/address combination which follows the data. Only three functional registers are shown in Figure 4-1. This is because the other two functional registers can only be used with the HP 86632A or HP 86633A AM/FM modulation section and these are not available with the synthesizer.

4.1.1.4 Interface Specifications

4.1.1.4.1. Remote Programming Connector

Remote programming commands are applied to the 8660B through a rear panel 36-pin blue ribbon connector labeled REMOTE INPUTS. Table 4-1 describes the functions of the various programming connector pins.

4.1.1.4.2 I/O Timing

A timing diagram showing the relationships of programming inputs and outputs is shown in Figure 4-2. It must be noted that there is also an ERROR signal output which is not shown in Figure 4-2. The ERROR signal is asserted by the HP 8660B when the programmed frequency is out of range. Since the user is expected to be aware of the frequency range of the synthesizer, this signal is not utilized in the implementation of the controller of the HP 8660B. The interested user must reference (4) for further information.

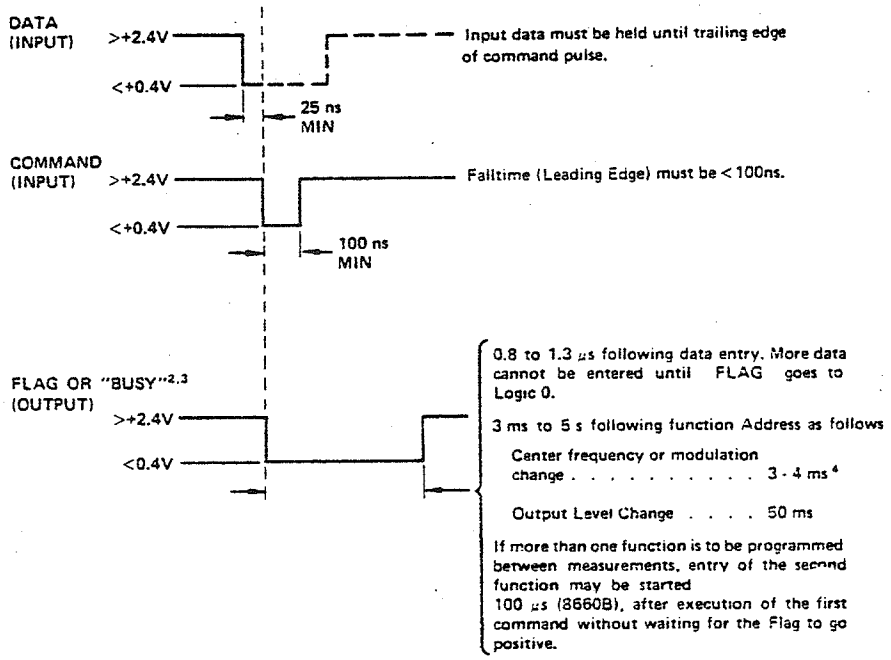
4.1.1.5 Controller (DEVICE 0)

4.1.1.5.1 Control Word Format and Programming Guide

Since the HP 8660B is not in the same room as the data acquisition system, therefore, the controller, apart from generating signals to program the HP 8660B, is also designed to trap the frequency programming code from the 7/32 and send

Table 4-1: REMOTE INPUTS Connector Description

J3 Remote Inputs Connector Pin Number	Function	Description
5	Local/Remote	Logic 1 (<0.4 V) puts instrument into REMOTE mode and disables front panel controls.
13	Digit 1-8	Data Entry Lines. 2 BCD coded digits entered simultaneously. LOGIC 1 = 0 V (< +0.4 V) LOGIC 0 = +5 V (> +2.4 V)
14	Digit 1-4	
15	Digit 1-2	
16	Digit 1-1	
28	Digit 2-8	
29	Digit 2-4	
30	Digit 2-2	
31	Digit 2-1	
9	COMMAND	Transfers input data into temporary register. When preceded by Qualifier/address, transfers data from temporary register to appropriate functional register and begins execution of programmed command. Data transfer occurs on leading edge of command pulse.
24	RESET	Logic 1 applied for 5 msec or more resets 8660B center frequency to 1.000000 MHz. (Does not affect frequency of 8660A.) For 8660A's and 8660B's with serial prefixes of 1335A or above this line also sets output attenuator to −140 dBm.
17	FLAG OR "BUSY" (Output from 8660A/B)	Signals receipt and execution of command. Flag will be at Logic 1 for 0.8 to 1.3 μsec during data entry or 3ms to 5sec following Qualifier/Address. See "I/O Timing" below. Output is open collector capable of current sinking 50 ma maximum.
3	ERROR (Output from 8660A/B)	Signals programmed frequency which is out of range of RF Section installed, or crystal oven not at temperature. Output is open collector capable of current sinking 50 ma maximum.
36	GROUND	Provides common ground connection between 8660A/B and programming source.
1 & 18	CONTINUITY	Pins are shorted together inside 8660 to allow programming source to verify continuity through connector.



[1] Flag output is open collector. To obtain levels shown connect output to +5 V power supply through approximately 1 kΩ load.

[2] After entering a Qualifier/Address combination, the Flag (Busy) line is held low for a period approximately equal to the execution time for the function programmed. In most cases actual execution will be faster than indicated by the Flag. However, in some special cases actual switching time may be longer than indicated by the Flag. See "Programming Execution Time" in (3).

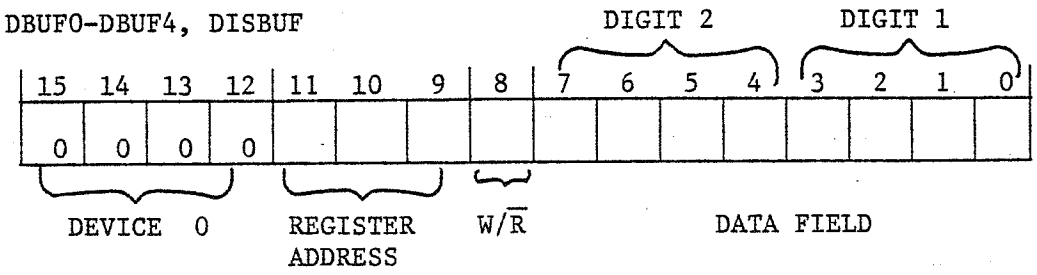
Figure 4-2: I/O Timing

the latched BCD code of frequency to the front panel display board. There it is decoded and displayed as a 10 digit 7-segment display on the front panel.

The controller has six buffer registers (address 000 - 101) and 1 control status register (address 110). Figure 4-3 gives the different word formats of these registers. The buffer registers DBUFO-DBUF4 (address 000 - 100) are for holding the 10 BCD digits for programming frequency (2 digits per register). It must be noted that the first four least significant bits of the buffer registers are called DIGIT 1 and the more significant four bits are called DIGIT 2. The buffer register DISBUF (address 101) is responsible for strobing the latched 10 BCD digits of frequency to the front panel display and must be loaded with the qualifier/address combination as discussed in section 4.1.1.3 of this chapter. The front panel display will only be changed during frequency programming, i.e., DIGIT 1 = 1111 (signifying execution) and DIGIT 2 = 0000 signifying frequency programming). All bits of the six buffer registers are "write-only" bits. The control status register DCSR controls the mode of the synthesizer (local/remote) and senses the FLAG output of the synthesizer. The FLAG (bit 1) will be at logical 1 when the synthesizer is busy and logical 0 when it is ready for data. Hence the user should "poll" the FLAG bit (bit 1) during programming. As can be seen in section 4.1.1.3 of this chapter, some functions do not require 10 BCD digits. However the user should still write into the buffer registers DB F 0 - DBUF 4 with the necessary number of digits as required by the function. These digits however will not be displayed due to a different function address being written into DIGIT 2 of DISBUF.

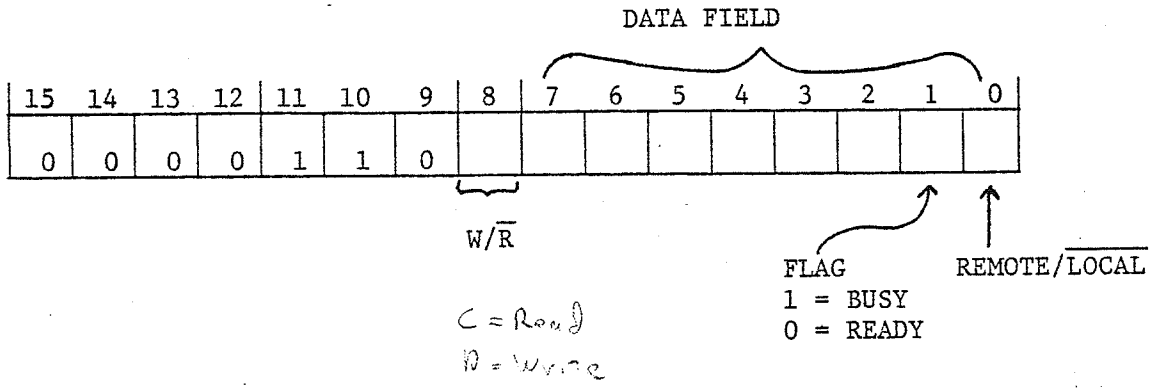
4.1.1.5.1 Controller Circuit Description

The controller consists of two boards, i.e., Board D3 (control logic, digit line driver and device address decorder) and Board D4 (carrier frequency display latch). Schematics are given in Figure A-2 of Appendix A. IC(AT) decodes bits



REGISTER NAME	REGISTER ADDRESS	DIGIT 2	DIGIT 1
DBUF 0	000	digit 1	digit 0
DBUF 1	001	digit 3	digit 2
DBUF 2	010	digit 5	digit 4
DBUF 3	011	digit 7	digit 6
DBUF 4	100	digit 9	digit 8
BISBUF	101	function address	qualifier (1111)

Figure 4-3(a): Buffer Register Control Word Format



BITS 0,1 = READ/WRITE

BITS 2-7 = NOT IMPLEMENTED

Figure 4-3(b): Control Status Register Control Word Format

12 to 15 of the 16 bit output of DIO 1 to enable device select. IC(AY), which is a 1 line to 8 line demultiplexor, routes a 400 ns "write strobing pulse" to enable writing into the different registers of the controller. The strobing pulse is derived from a one-shot IC(BY). IC(BY) is triggered under the condition DEV 0 • W • DOPDA. DEVO is a signal derived from decoding the four most significant bits of the DIO. DEV 0 is asserted if the synthesizer is addressed by the 7/32 computer. The 400 ns pulse generated by IC(BY) is inverted by IC(BW) and serves as a command pulse to the HP 8660B synthesizer. Bit 1 of DCSR (the FLAG bit) is set by the output of IC(BY) strobing IC(CY). When pin 5 of IC(CY) is logical 1, the synthesizer is busy. IC(CY) is reset by a rising edge from the FLAG output of the HP 8660B. A rising edge of the FLAG output indicates that the HP 8660B is ready and hence a logical 0 of bit 1 of DCSR indicates a ready condition of the HP 8660B. The 1 kΩ at pin 3 of IC(CY) is necessary because the FLAG output of the HP 8660B is an open-collector type output. Bit 0 of the DCSR is latched by IC(DY) and the clocking pulse is derived from the Y6 output of IC(AY). Since the HP 8660B accepts negative logic, IC(BW) is used to invert the Q output (pin 5) of IC(DY) to generate LOCAL/REMOTE to the HP 8660B. Only bit 0 and bit 1 of DCSR can be read back through the 16 bit input of DIO 1. This is accomplished by enabling IC(CW) by the output (pin 10) of IC(AX) which goes low during read mode and when DCSR is addressed. IC(CW) is a tri-state inverting driver. An inverting driver is used because the 16 bit input of DIO 1 accepts negative logic. Provisions are made to automatically clear the flip-flop of IC(DY) which latches bit 0 of DCSR during power-up. This makes sure that the HP 8660B is in local mode initially. Output bits 0 - 7 are inverted by IC(BW) and IC(CW) because the HP 8660B accepts negative logic. The two BCD digits, i.e., OBIT 0 - OBIT 7, LOCAL/REMOTE and FLAG are connected to the

Remote Inputs Connector J3 of the HP 8660B via connectors AA0 and AA4.

The carrier frequency display latch is implemented by two level latches. IC's (A0), (A1), (A2), (A3), and (A4) make up the first level and IC's (B0), (B2), (B3), and (B4) make up the second level. IC's (A0), (A1), (A2), (A3), and (A4) actually constitute DBUF 0 - DBUF 4. Each of these latches latch two BCD digits and the strobing pulses are derived from the outputs of IC(AY) on Board D2. These pulses are routed from Board D2 via connectors AA1 and AA2. The latched ten BCD digits will be strobed into the second level latch when 00001111 is written into DISBUF. This two level latch implementation makes sure that the front panel "Carrier Frequency" display does not flicker during transients.

4.1.2 Programmable Window Generator

4.1.2.1 Device Description

This device is responsible for generating a window coherent with the signal output of the HP 8660B synthesizer. This device can generate a window with a duty cycle equivalent to 0.5, 1, 2, 4, 8, 16, 32, 64, and 128 cycles of the synthesizer signal. The window trigger can be either CPU or manually controlled. In the CPU controlled mode, the 7/32 can either generate a single shot trigger or a continuous trigger. In the manual mode a single shot trigger is generated by a push button switch on the system front panel or a continuous trigger can be selected by a manual repetition frequency select switch on the system front panel. In both modes, the continuous trigger has a repetition frequency of 8000, 4000, 2000, 1000, 800, 400, 200, or 100 Hz.

A block diagram of the programmable window generator is given in Figure 4-4 (a) and (b). The generator is contained in boards A0, A1, A2, and A3. The sine wave output of the HP 8660B synthesizer is shaped into a square wave (TTL level)

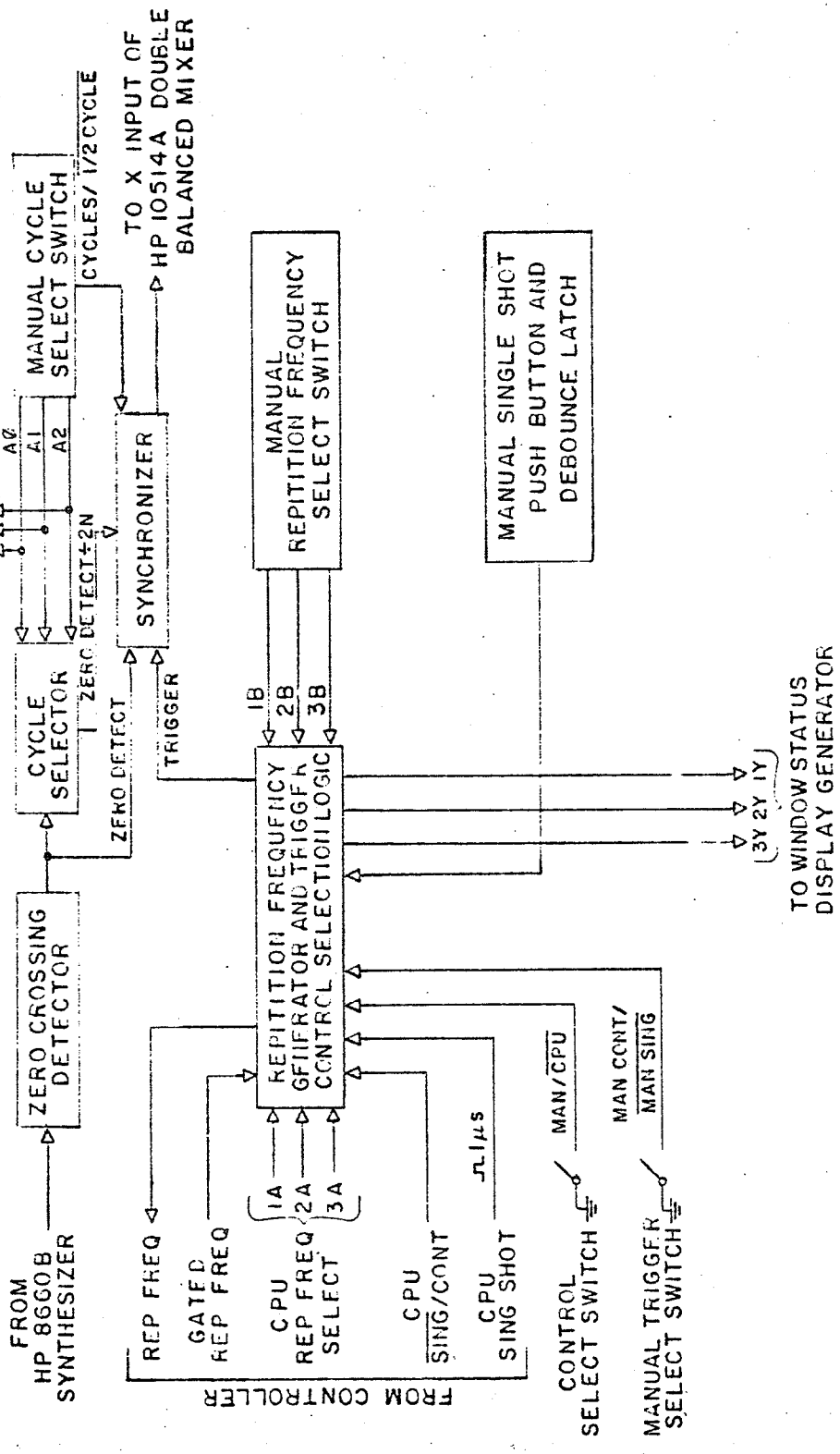


Figure 4-4(a): Programmable Window Generator Block Diagram

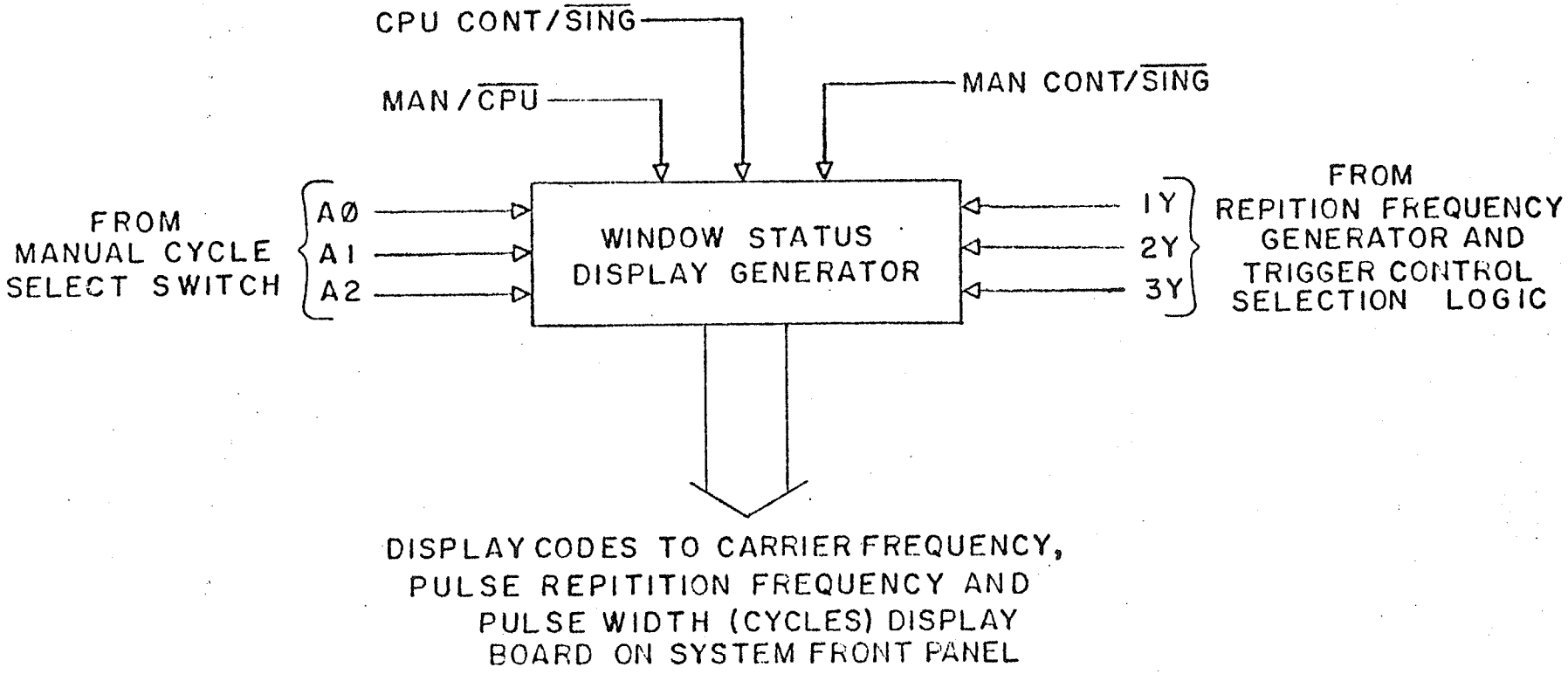


Figure 4-4(b): Window Status Display Generator of the Programmable Window Generator

by the zero crossing detector. This signal (ZERO DETECT) is then divided down by synchronous counters in the cycle selector. The binary code generated by the manual cycle select switch then selects the different divided signal (ZERO DETECT $\div$ 2N, where N = number of cycles that the window width to be equaled to, and N = 1, 2, 4, 8, 16, 32, 64, and 128). ZERO DETECT and ZERO DETECT $\div$ 2N are then fed into the synchronizer which is the main window generating device. Both the ZERO DETECT and ZERO DETECT $\div$ 2N are asynchronous to the TRIGGER and CYCLES /$\overline{\text{½ CYCLE}}$ will select between ZERO DETECT and ZERO DETECT $\div$ 2N to be used for the window generation. It must be noted that the duty cycle of these two signals are equivalent to the different widths that is required of the window generated. The synchronizer essentially "synchronizes" the trigger with either ZERO DETECT or ZERO DETECT $\div$ 2N, depending on which ever is selected by CYCLES/$\overline{\text{½ CYCLE}}$, and generates a window (with width equivalent to the "high" portion of either ZERO DETECT or ZERO DETECT $\div$ 2N) on every rising edge of the trigger input. This window will then drive the X input of the HP 10514A double balanced mixer.

The repetition frequency generator and trigger selection logic provides a trigger, which can be a single shot or a continuous pulse train, to the synchronizer. The trigger can be either CPU (7/32) or manually controlled. During CPU control, the CPU can select between the single shot or continuous trigger mode, generate the single shot, select the repetition frequency of the continuous trigger and start the trigger by gating the repetition frequency. During manual mode, the trigger will be free running during continuous trigger mode. Controls such as continuous/single shot select, single shot and repetition frequency select are done by the different manual switches as can be seen on the block diagram.

The window status display generator accepts inputs from the repetition frequency generator and trigger control selection logic and the manual cycle select

switch and generates BCD codes to the carrier frequency, pulse repetition frequency and pulse width (cycles) display board. The display board displays the pulse repetition frequency and number of cycles of sine wave in the tone burst signal generated. The window status display generator will also display mode information such as CPU/manual control and single-shot/continuous trigger on the system front panel.

4.1.2.2 Circuit Description

4.1.2.2.1 Zero crossing detector

This is the wave shapping device located on Board A2 (Figure A-3(a) of Appendix A) converting the HP8660B synthesizer sine wave output into a square wave TTL signal. Due to the high frequency sine wave output (1 MHz - 50 MHz) of the synthesizer, an ECL voltage comparator (Advanced Micro Device's AM 685) is used as the zero-crossing detector element. The ECL level output of the Am 685 is then converted into TTL level by the ECL to TTL level translator (Motorola's MC 10125). The Am 685 switches at 5 mV overdrive. The $\overline{Q}$ output of the Am 685 is used and the non-inverting input (pin 3) is biased to 50 mV to prevent erronous switching due to possible noise. The 5.1 kΩ feedback resistor from the Q output to the non-inverting input provides some hysteresis to the comparator circuit. The input to the inverting input is AC coupled by the 0.001 μF and 1 kΩ. The matching T network at the input provides a 50 Ω load to the HP 10514A double balanced mixer. The T network also seves as an attenuator cutting the signal to the mixer to 0.5 V_{o-p} when the synthesizer is programmed to give an output of 1 V rms.

4.1.2.2.2 Cycle Selector

The cycle selector, located on Board A3 (Figure A-3(d) of Appendix A), basically accepts the output (ZERO DETECT) from the xero crossing detector and divides ZERO DETECT down into eight different frequencies by a two stage synchronous counter IC(BX) and IC(CX). These different divided-down signals are then selected by a multiplexor IC(AX) which has its select input derived from the manual cycle select switch. The output of this circuit, ZERO DETECT $\div$ 2N, is then routed to the synchronizer circuit. IC(AY) serve as drivers for the three on-board LED's to indicate the frequency selected. The select input from the manual cycle slect switch is routed to the window status display generator to generate BCD codes for pulse width (number of cycles) to be displayed on the system front panel.

4.1.2.2.3 Manual Cycle Select Switch

Located on Board A3 (Figure A-3(e) of Appendix A), this switch generates codes to the cycle selector to select the different divided-down signals (ZERO DETECT $\div$ 2N) and a select signal (CYCLES/$\overline{\text{½ CYCLE}}$) to the synchronizer to select between ZERO DETECT and ZERO DETECT $\div$ 2N. IC(AZ) is a priority encoder generating the binary select codes to the cycle selector. It must be noted that the nine position switch also has two pole pieces for selecting the two delay lines for delaying the synthesizer output before going into the L input of the double balanced mixer.

4.1.2.2.4 Synchronizer

The synchronizer is the main window generating device of the programmable window generator. This is located on Board A3 (Figure A-3(f) of Appendix A).

This "synchronizes" the TRIGGER input with the ZERO DETECT or ZERO DETECT ÷ 2N. The window generated will have a width equivalent to the "high" part of a cycle of ZERO DETECT or ZERO DETECT ÷ 2N depending which is selected by CYCLES/$\overline{½ \text{ CYCLE}}$. A single window is generated for every rising edge of the TRIGGER.

A rising edge on trigger will set the first flip-flop on IC(BY). Pin 8 of IC(BY) goes to logic 0. Output pin 4 of IC(CY) will go to logic 1 when the output (pin 4) of IC(EY) is at logic 0. Output of IC(CY) then sets the second flip-flop of IC(BY). Pin 5 of IC(BY) will go high. Output (pin 3) of IC(DY) will go high when pin 4 of IC(EY) goes high. Should pin 4 of IC(EY) go to logic 0, pin 3 of IC(DY) also goes to logic 0. A window is thus generated with a width equivalent to the "high" part of a cycle of the signal at the output of the multiplexor IC(EY). When pin 3 of IC(DY) goes to logic 0, the two flip-flops of IC(BY) are cleared to prevent window generation and a second window can only be generated by a second rising edge on the TRIGGER signal. The window is routed to output (pin 6) of the 50 Ω line driver IC(DX). The output of IC(DX) is dropped to 2.4 V_{o-p} by the four series diodes. The single diode parallel to the four series diodes eliminates any possible undershoot. The 2.4 V_{o-p} is further divided down by the resister divider 180 Ω and 75 Ω to 0.32 V_{o-p}. The 180 Ω and 75 Ω comination also makes sure the mixer X input sees a 50 Ω load. The 0.32 V level is essential in order not to exceed the input power limit of the double balanced mixer.

4.1.2.2.5 Repetition Frequency Generator and Trigger Control Selection Logic

The repetition frequency generator, on Board A1 (Figure A-3(h) of Appendix A) consists of a time base derived from an 8 kHz crystal oscillator. This 8 kHz reference is divided down by IC's (CX), (BX), (AX), (DY), and (CY) into 4 kHz, 2 KHz, 1 KHz, 800 Hz, 400 Hz, 200 Hz and 100 Hz. These different frequencies

together with the 8 kHz reference serve as continuous triggering sources to the synchronizer circuit. These eight different frequencies are selected by the multiplexor IC(BY) with select input derived from the three bit binary outputs of IC(AY). IC(AY), which is a quadruple 2 to 1 multiplexer selects the above mentioned three bit binary output either from the manual repetition frequency select switch output or from the CPU. The select input to IC(AY) is derived from the control select switch on the system front panel. IC(CZ) selects between continuous and single shot trigger during CPU control mode and IC(EZ) selects between continuous and single shot trigger during manual control mode. The outputs (pin 4) of IC's(CZ) and (EZ) are connected to pin 14 and 13 respectively of the fourth multiplexor of IC(AY). The 4Y output (pin 12) of IC(AY) thus provides a trigger (single shot or continuous) either controlled by the CPU or manually to the synchronizer board. The GATED REP FREQ to pin 3 of IC(CZ) is actually REP FREQ at pin 5 of IC(BY) gated by an on/off signal in the controller for the window generator. The three on-board LED's are driven by IC(DZ) and provides indication of the REP FREQ selected.

4.1.2.2.6 Manual Repetition Frequency Select Switch

This is an eight position switch on the system front panel enabling the user to select the pulse repetition frequency during the manual control mode. The switch circuit is located on Board A1 (Figure A-3(i) of Appendix A). A three bit binary select code is generated by IC(BZ) depending on the switch position. This three bit code will go to IC(AY) and will be used to select the required REP FREQ during mannual control mode.

4.1.2.2.7 Manual Single Shot Push Button and Debounce Latch

This is a push button on the system front panel which generates a single rising edge to the synchronizer circuit for every push. The switch circuit is located on Board A3 (Figure A-3(g) of Appendix A). The single rising edge is generated by the latching circuit of IC(AY) to eliminate switch bounce.

4.1.2.2.8 Window Status Display Generator

This circuit generates BCD codes for pulse repetition frequency and pulse width (cycles) information to be displayed on the carrier frequency, pulse repetition frequency and pulse width (cycles) display board on the system front panel. It also causes control mode (i.e., CPU/manual) and trigger mode (i.e., single shot/continuous) to be displayed on the system front panel by lighting up LED's. The circuit is located on Board AO (Figure A-3(j), (k), (l), and (m) of Appendix A).

The different pulse repetition frequencies are 8000, 4000, 2000, 1000, 800, 400, and 100 MHz. The pulse repetition frequency display code is generated as a result of decoding the three bit binary select code from IC(AY) of the repetition frequency generator and trigger control selection logic (Board Al). The two least significant bits, i.e., 2Y and 1Y act as select inputs to IC(BV) and IC(BW) generating 1000_2, 0100_2, 0010_2, and 0001_2. The most significant bit 3Y will act as select input to IC's(CV) and (CW) choosing whether to use the outputs of IC's(BV) and (BW) or forcing a 0000_2 to Digit 3 and Digit 2. The two least significant digits, i.e., Digit 0 and Digit 1 are always zero and hence they are always forced to zero.

The different pulse width (cycles), i.e., window widths are 128, 64, 32, 16, 8, 4, 2, 1, and 0.5. CYCLES/$\overline{\frac{1}{2}\ \text{CYCLE}}$, which is generated by the manual cycle

select switch, selects between 0.5 cycles and 1.0 or more cycles. This thus serves as a select input to IC(AT) choosing to generate either a 0 or a 5 for Ditit 0--the first digit after the decimal point. The three bit binary select codes A2, A1, and A0 are decoded by IC's(AV), (AW), (AX), and (AY) to generate Digit 1. The output codes of IC's(AV), (AW), (AX), and (AY) are 8, 4, 2, 6, 8, 4, 2, and 1 if CYCLES/$\overline{\frac{1}{2}\ \text{CYCLE}}$ = 1 and 0 if CYCLE/$\overline{\frac{1}{2}\ \text{CYCLE}}$ = 0. When A2 = 1 and CYCLES/$\overline{\frac{1}{2}\ \text{CYCLE}}$ = 1, codes will be generated by IC's(BX) and (BY) to make Digit 2 = 2, 6, 3, or 1 and Digit 2 = 0 otherwise. Digit 3 will be equal to 1 only if A2 = A1 = A0 = CYCLE/$\overline{\frac{1}{2}\ \text{CYCLE}}$ = 1.

The mode information, i.e., manual/CPU control and continuous/single shot trigger are generated by decoding MAN/$\overline{\text{CPU}}$, CPU CONT/$\overline{\text{SING}}$ and MAN CONT/$\overline{\text{SING}}$ from the trigger control selection logic and displaying the mode information by lighting up LED's on the system front panel.

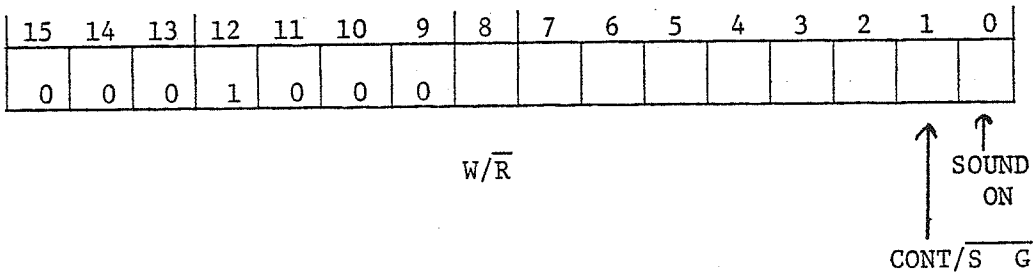
4.1.2.3 Controller (DEVICE 1)

4.1.2.3.1 Control Word Format and Programming Guide

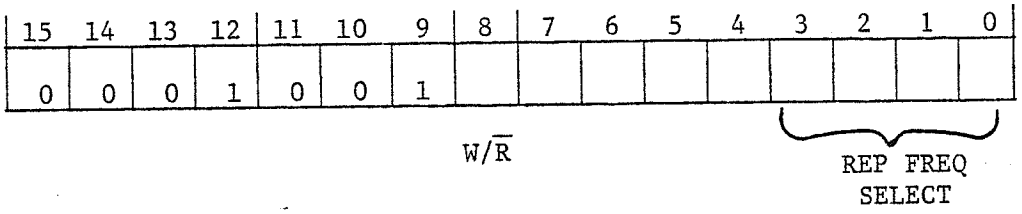
The controller has one control status register WCSR (addr = 000) and one buffer register WBUF (addr = 001). All bits of WCSR are write-only bits and only bits 0 and 1 are implemented. A logical 1 on bit 0 will turn on the continuous trigger (provided bit 1 is at logical 1). Should a logical 0 be written into bit 1, a 1 μs single shot will be generated to trigger the synchronizer circuit regardless of the state of bit 0.

WBUF programs the pulse repetition frequency by writing into bits 0, 1, and 2 (read/write bits). Figure 4-5 gives the control word formats of the controller.

WCSR (read/write)
Addr = 000



WBUF (read/write)
Addr = 001



Bits 2	1	0	Rep Freq (Hz)
0	0	0	100
0	0	1	200
0	1	0	400
0	1	1	800
1	0	0	1000
1	0	1	2000
1	1	0	4000
1	1	1	8000

Figure 4-5: Control Word Format for Programmable Window Generator (DEVICE 1)

4.1.2.3.2. Controller Circuit Description

The controller circuit is located on Board D5 (Figure A-4 of Appendix A). IC(AY), which is a demultiplexor, routes the strobing pulse DOPDA to one of its outputs Y0 and Y1. A negative pulse occurs at pin 15 of IC(AY) when DEV 1 • $W/\overline{R}$ • $\overline{\text{OBIT 9}}$ • $\overline{\text{OBIT 10}}$ • $\overline{\text{OBIT 11}}$ = 1. This causes IC(AX) to latch bits 0 and 1 of WCSR. A logical 1 on bit 0 turns the GATED REP FREQ on and provides a continuous trigger to the synchronizer of the programmable window generator provided bit 1 of WCSR is also set to a logical 1. During CPU single shot mode, a "0" is written into bit 1 of WCSR and pin 6 of IC(AX) goes "high." A 1 μs pulse (pin 13 of IC(CV)) is triggered by the Y0 output of IC(AX) and the pulse is gated to pin 6 of IC(CX) and routed to the window generator circuit as a single shot trigger. The 1 μs CPU SINGLE SHOT also triggers a 500 ms single shot (pin 5 of IC(CV)). This pulse provides a long enough turn-on duration for the SOUND ON LED to be visually detected by the user. The SOUND ON LED will also be turned-on when bit 0 of WCSR is "high." Bit 0 and 2 of WBUF are latched by IC(BW).

During read mode, IC(BY) acts as a decoder decoding the read condition and turns on the corresponding drivers on IC(AW) to enable the addressed register to be read.

4.1.2.4 Performance Evaluations

With the synthesizer programmed to give an output of 1 V_{o-p} the window generator produces a window at 0.32 V_{o-p} into 50 Ω. The window has a 15 ns rise-time and 10 ns fall-time at all frequencies. It was observed that there is a frequency limitation in every cycle selection and should the maximum frequency be exceeded, multiple windows will be generated. This limitation is due to the fact that time is required to clear the window generating flip-flops in the

synchronizer circuit. A summary of the window frequency limitation is given in Table 4-2. Figure 4-6 gives a scope trace of a typical window. The window is delayed 30 ns late at 0.5 cycle window width and 42 ns at all other cycle selections. Two delay lines, i.e., 30 ns and 42 ns are then used to delay the snythesizer signal to match with the window zero-crossing. The window is further tested by mixing the window and the delayed synthesizer sine wave output with HP 10514A double balanced mixer. The mixer output (the R terminal) is terminated with a 50Ω load and monitored with a scope. Figure 4-7 shows typical tone burst signals generated.

Table 4-2: Frequency Limitations of Programmable Window Generator

CYCLES	MAX OPERATION FREQ (MHz)
0.5	10
1.0	25
2.0	45
4.0	50
8.0	50
16.0	45
32.0	49
64.0	47
128.0	*40

*At 8 kHz pulse repetition frequency, operation frequency is 2 MHz - 40 MHz.

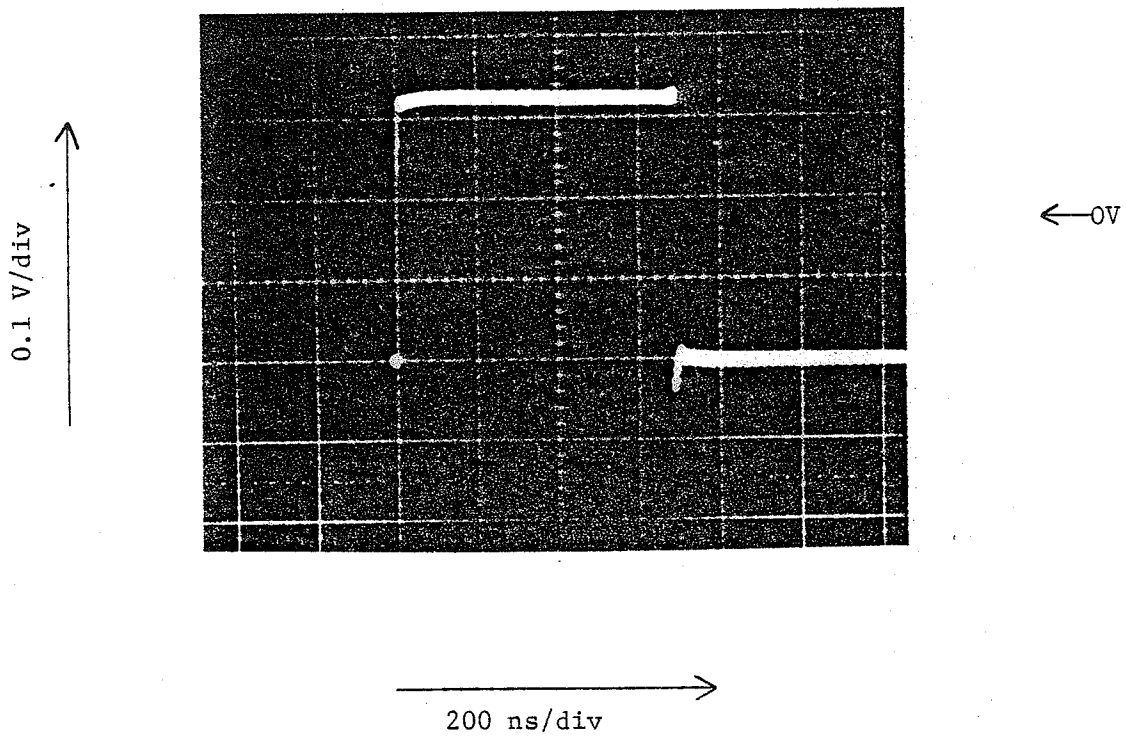
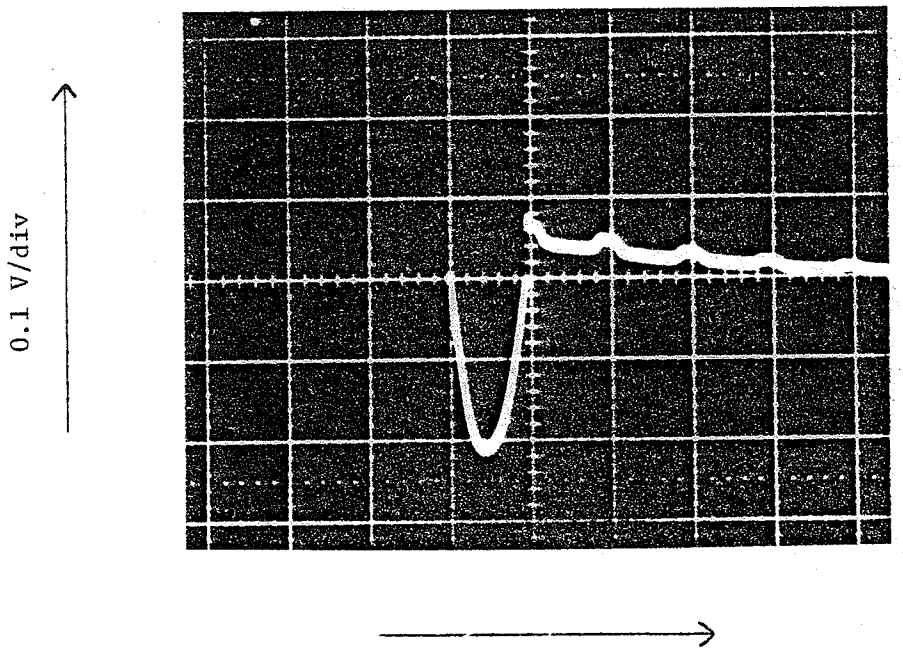


Figure 4-6: A Typical Window



0.5 CYCLE 1 MHz 8000 Hz PRF

Figure 4-7(a): Broad Band Pulse

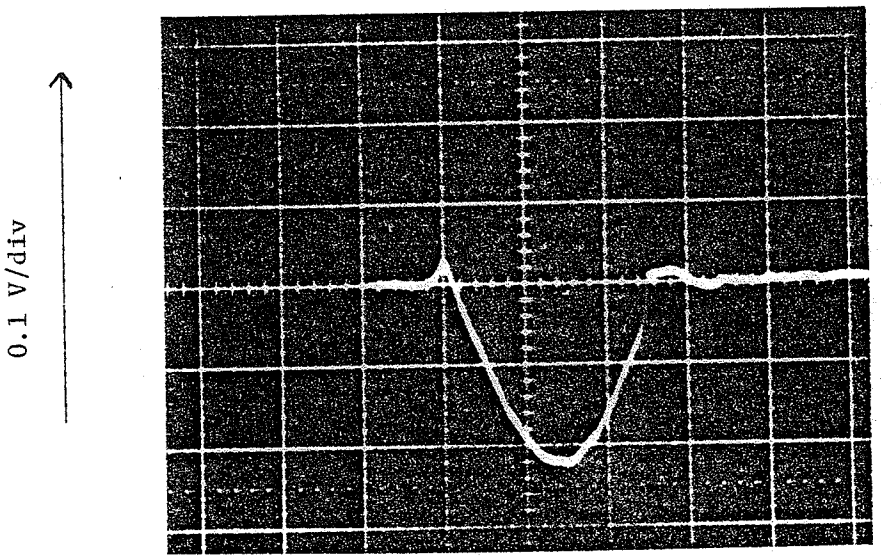


Figure 4-7(b): Broad Band Pulse

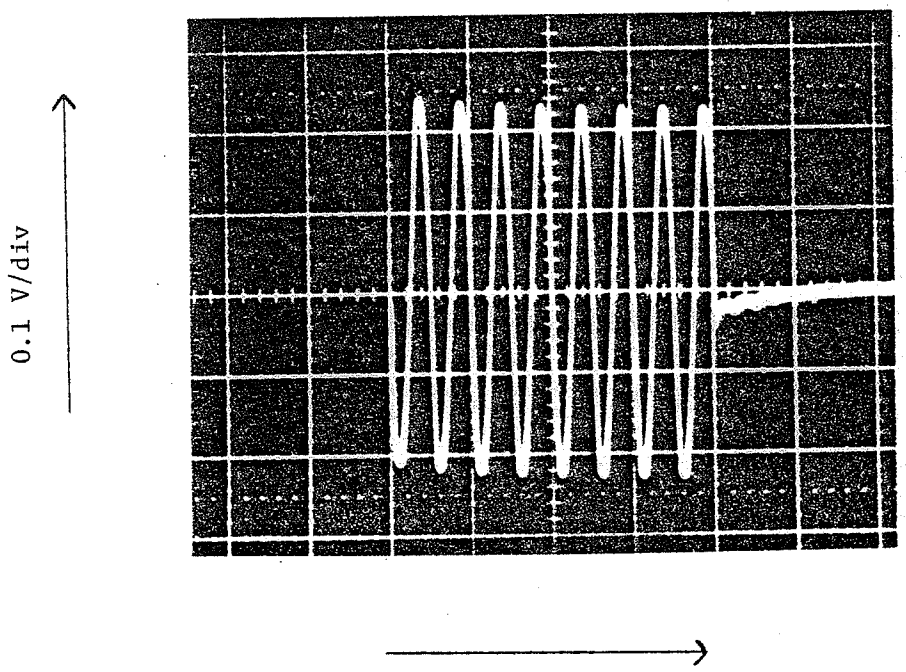


Figure 4-7(c): Coherent Tone Burst

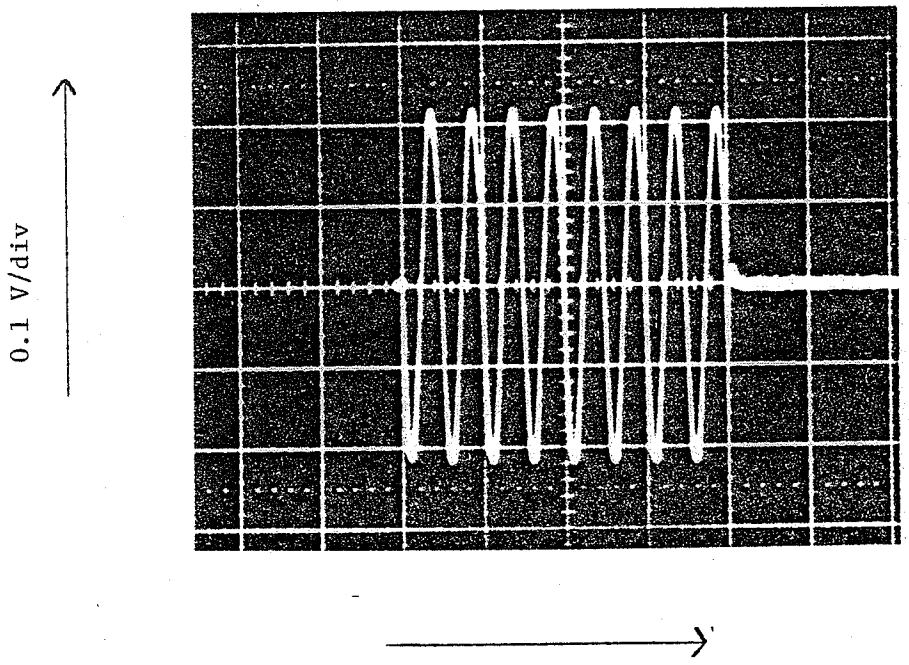


Figure 4-7(d): Coherent Tone Burst

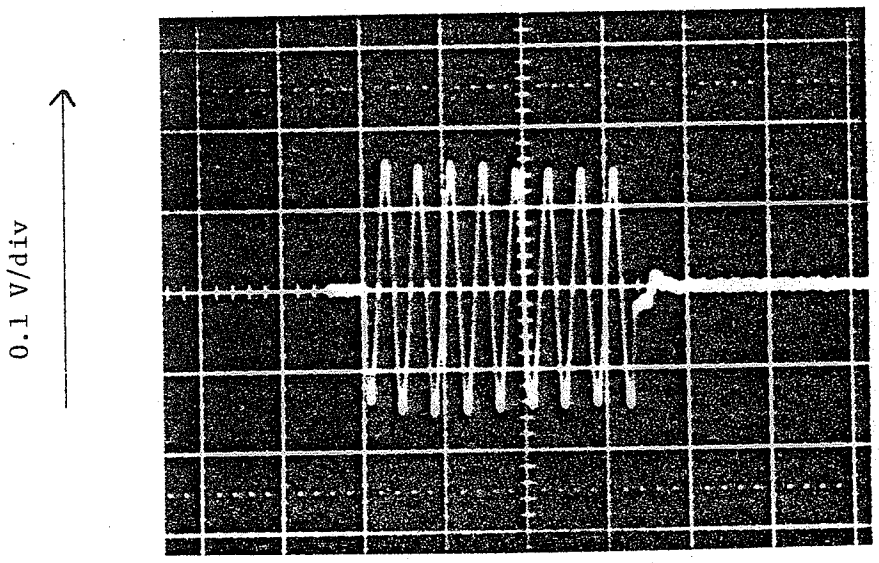


Figure 4-7(e): Coherent Tone Burst

4.1.3 Delay Lines 1 and 2

4.1.3.1 Device Description

These are RG-174/U coaxial cables trimmed to give a signal delay of about 30 ns for delay 1 and 42 ns for delay 2. These delay lines are used to delay the synthesizer signal in order to match the zero-crossing of the synthesizer signal with the zero-crossing of the window. Delay 1 is used when half a cycle of a sine wave is transmitted and delay 2 is used with the other cycle selections of the programmable window generator. The switch which selects these delays is part of the manual cycle select switch (4 pole, 9 positions) on the system front panel.

4.1.4 Double Balanced Mixer

4.1.4.1 Device Description

The HP 10514A double balanced mixer is used. This device is responsible for generating a tone burst signal at its R output terminal by accepting a 0.32 V_{o-p} window at the X input and a delayed sine wave signal (from the HP 8660B synthesizer) at the L input. The tone burst signals are coherent as a result of the properties of the programmable window generator. Scope traces of tone-burst signals are given in the performance evaluation section of the programmable window generator. Input limitations are 5 mW into 50 Ω at the L input and 50 mA maximum into 50 Ω at the X input. The T network at the input to the zero-crossing detector circuit of the programmable window generator serves as an attenuator to cut the sine wave signal to the L input of the mixer to 0.5 V_{o-p} should the synthesizer be programmed to give a maximum output of 1 V_{rms}. It was observed during the testing process of coherent tone burst generation that the synthesizer should be programmed to give a 1 V (zero to peak) output because higher voltages

will cause the signal peaks of the tone burst generated to clip. From the specification sheet (reference (6)), this mixer has an on/off ratio of 35 dB.

4.1.5 Programmable Attenuator

4.1.5.1 Device Description

The programmable attenuator is responsible for varying the fixed amplitude tone-burst signal of the R output of the double balanced mixer. The attenuator is implemented by an R-2R ladder network similiar to a digital-to-analog converter (DAC). A description of a general n-bit DAC implemented by a R-2R ladder network is as follows. A schematic of the n-bit DAC is shown in Figure 4-8. Since the ladder is linear, superposition can be used for anlaysis. Consider the $(n-1)^{th}$ switch (MSB) at V_R and all other switches at 0V. The resistance at the $(n-1)^{th}$ node looking to the left is 2R since the input terminal of the operational amplifier is at virtual ground. The resistance at any node looking in either direction of the ladder network is 2R, provided the end nodes of the network are terminated by 2R. Hence the voltage at the $(n-1)^{th}$ node as a result of the contribution of the $(n-1)^{th}$ voltage only as shown in Figure 4-9(a) is given by

$$V_{n-1} = V_R\left(\frac{R}{3R}\right) = \frac{V_R}{3} \tag{4-1}$$

where V_R is the refernce voltage. Since the gain of the operational amplifier, with respect to node n-1 was chosen to be $-\frac{3}{2}$ ($R_f = 3R$ in Figure 4-8), the output voltage due to the MSB alone is

$$V_{out}(MSB) = \left(\frac{V_R}{3}\right)\left(\frac{-3}{2}\right) = \frac{-V_R}{2} \tag{4-2}$$

Consider next switch A_{n-2} at V_R with all other switches at 0 V (see Figure 4-9(b)).

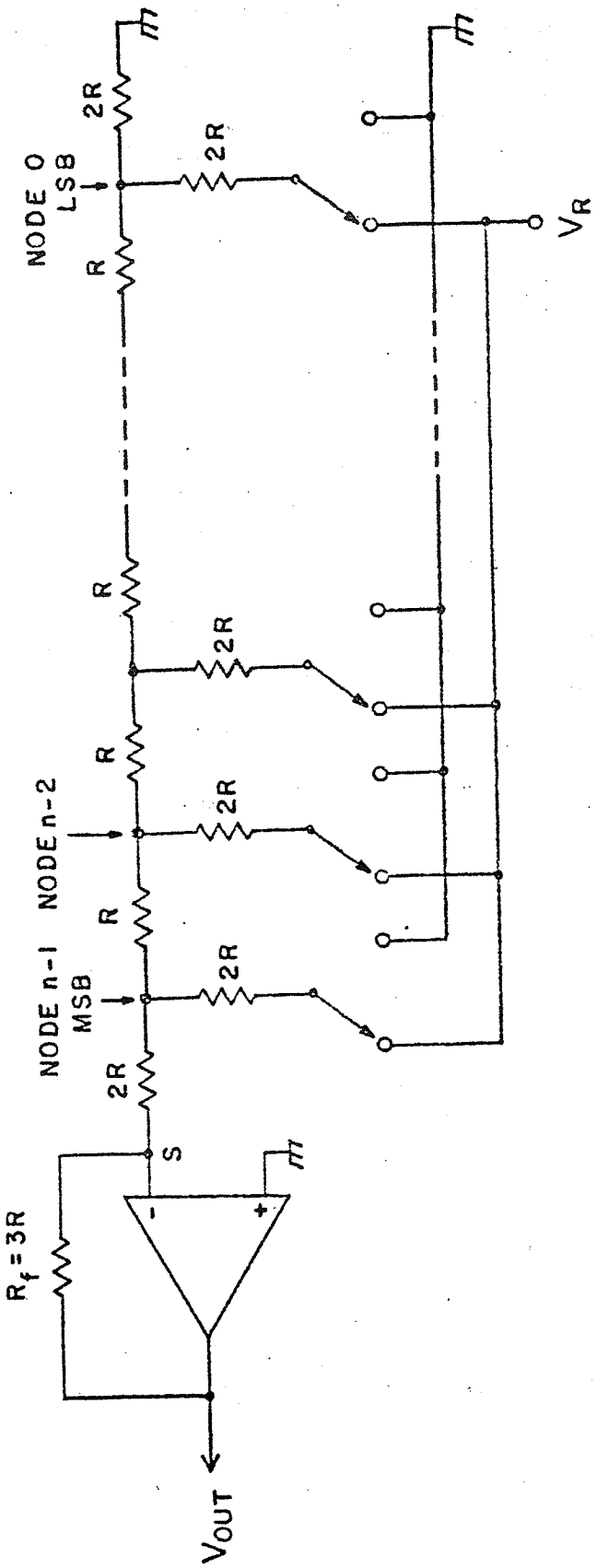


Figure 4-8: A General n-bit Digital-to-analog Converter

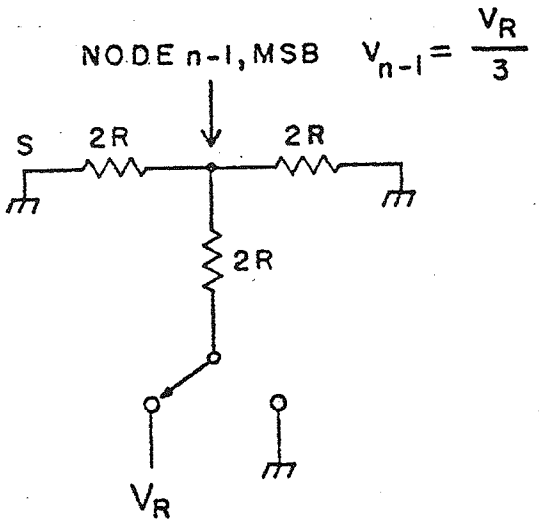


Figure 4-9(a): Voltage at the $(n-1)^{th}$ Node with the $(n-1)^{th}$ Switch at V_R

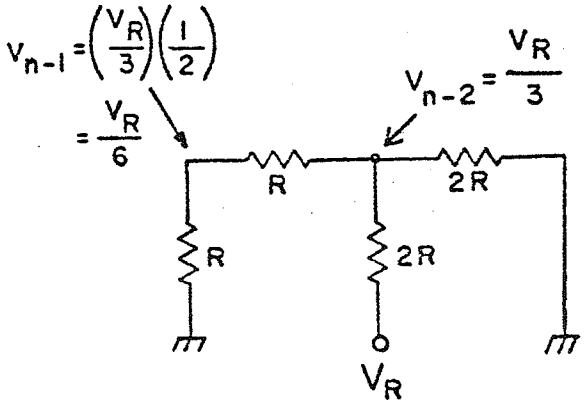


Figure 4-9(b): Voltage at the $(n-2)^{th}$ Node with the $(n-2)^{th}$ Switch at V_R

a similar situation exists. That is, the equivalent resistance to the left and right of node n-2 are 2R and the resulting voltage at node n-2 is

$$V_{n-2} = \frac{V_R}{3} \tag{4-3}$$

This voltage is attenuated by a factor of 2 at node n-1 as is shown in the equivalent circuit of Figure 4-9(b). Thus, its contribution to the output at the operational amplifier is

$$V_{out}(\text{due to node n-2}) = (\frac{V_R}{3})\ (\frac{1}{2})\ (\frac{-3}{2}) = \frac{-V_R}{4} \tag{4-4}$$

The same procedure applied to the remaining node yields

$$V_{out} = -V_R(A_{n-1}\ 2^{-1} + A_{n-2}\ 2^{-2} + \ldots + A_1 2^{-(n-1)} + A_o 2^{-n}) \tag{4-5}$$

Where A_i = 0 or 1, depending on whether the i^{th} switch is at 0V or at V_R, respectively. Thus the output of the D/A converter is proportional to the sum of the weights represented by those switches that are connected to V_R.

In the implementation of the programmable attenuator, a tone-burst signal from the double balanced mixer, is used for V_R. A total of six switches is used. Thus the attenuator is capable of attenuating the fixed constant output of the double balanced mixer in 64 steps with a dynamic range of 36 dB. However, in the actual usage, the attenuator will only be used to vary its attenuation in factors of two. The output singal is reinverted by another inverting amplifier and thus the output voltage of the attenuator is given by

$$V_{out} = V_{BURST}(A_5 2^{-1} + A_4 2^{-2} + A_3 2^{-3} + A_2 2^{-4} + A_1 2^{-5} + A_o 2^{-6}) \tag{4-6}$$

where V_{BURST} is the output voltage of the double balanced mixer. An advantage of

using the R-2R ladder network implementation is the capability of fine tuning and ease of programming the device.

Due to the toggling of the switches at the R-2R ladder network, the effective input impedance into the ladder network changes with different switch positions. A buffer amplifier is thus used to buffer the double balanced mixer output. The input to the buffer amplifier is terminated at 50 Ω to ground to match the output impedance of the double balanced mixer.

4.1.5.2 Circuit Description

The attenuator is implemented almost exactly as the DAC of Figure 4-8 (see Figure A-5 of Appendix A). In addition to the implementation of Figure 4-8, an inverting amplifier is put at the output of the DAC to invert the signal back to positive polarity and a high current drive buffer amplifier (identical to the buffer amplifier at the input to the R-2R ladder) is used at the output to provide a 50 Ω load driving capability. This buffer amplifier is essential because the L input of the HP 10514A double balanced mixer has a 50 Ω input impedance. In the ladder implementation, R = 301 Ω, 2R = 601 Ω, and 3R = 903 Ω. Analog switches (Siliconix's DG 190A) are used and these switches have an "ON" resistance of 30 Ω. Hence the 2R branch connecting to the switches are formed by R_1 = 150 Ω and R_2 = 422 Ω which together with the switch "ON" resistance will make up 2R = 601 Ω. These switches have the advantage of low "ON" resistance, capable to switch video signals and "break-before-make" action. All resistors are 1% metal film resisters to minimize error due to unequal resistance at the branches of the R-2R ladder. All resistance values are made below 1 kΩ since a 2 pF stray capacitance will cause a "roll-off" at about 80 MHz. Also, higher resistance values will cause "roll-off" at lower frequencies. The control bits A_5, A_4, A_3,

A_2, A_1, and A_0 are TTL inputs which originate from the controller of the attenuator. The AM 500 has a gain bandwidth of 100 MHz and the buffer amplifier LH 0063CK has a bandwidth of 200 MHz.

4.1.5.3 Controller (DEVICE 2)

4.1.5.3.1 Control Word Format and Programming Guide

Since the attenuator has only six control bits, the controller has only one buffer register ABUF (addr = 000). Only the first six bits of ABUF are implemented. All bits are read/write bits. All reading and writing operations follow the general read/write procedure as mentioned in section 3.2 of Chapter 3. Figure 4-10 gives the control word format for ABUF.

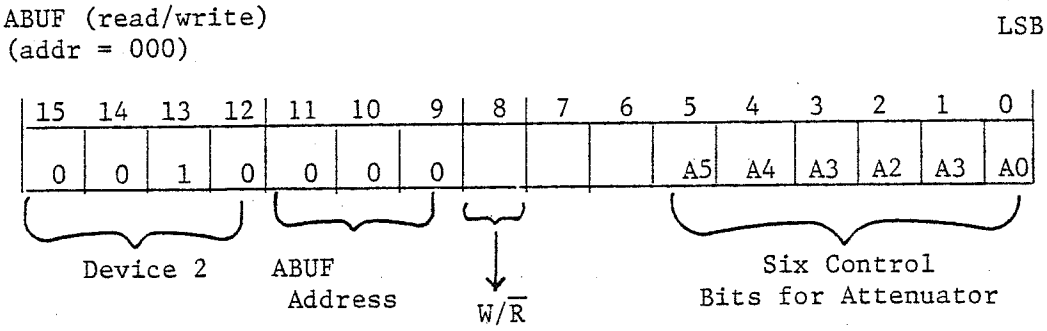


Figure 4-10: Control Word Format for the Programmable Attenuator.

4.1.5.3.2 Controller Circuit Description

The controller for the attenuator shares the same board D5 as the controller for the Programmable Window Generator. The schematics of the controller is given in Figure A-6 of Appendix A. $\overline{\text{DEV 2}}$ originates from the Device Address Decorder on Board D2 (HP 8660B Controller). IC(BT), which is a demultiplexor, routes a 1 μs strobe pulse (DOPDA) to strobe in the six control bits to IC(BV). IC(BV)

is a six bit D-type register. The 1 μs strobe pulse is routed to strobe IC(BV) under the condition DEV 2 • $\overline{(\text{OBIT 9})}$ • $\overline{(\text{OBIT 10})}$ • $\overline{(\text{OBIT 11})}$ • WRITE. During read mode, IC(CT) acts as a decoder decoding the read condition, i.e., DEV 2 • $\overline{\text{OBIT 9}}$ • $\overline{\text{OBIT 10}}$ • $\overline{\text{OBIT 11}}$ • READ. During read mode, pin 15 of IC(CT) therefore goes "low" and subsequently turns on IC(AV). IC(AV) is a tri-state driver driving the 16 bit input of DIO 1. It must be noted that the signals $W/\overline{R}$ • DOPDA and $\overline{W/\overline{R}}$ originates from the Programmable Window Generator control logic on the same Board D5.

4.1.5.4 Performance Evaluation

The programmable attenuator was tested by feeding a 1 V_{o-p} signal from the HP 8660B Synthesizer to the input of the buffer amplifier before the programmable attenuator. The input to the buffer amplifier is terminated with 49.9 Ω resistor. The output of the attenuator is terminated with a 49.9 Ω load and monitored on an oscilloscope. Frequency responses of each of the control a bits, i.e., A_0, A_1, A_2, A_3, A_4, and A_6 were obtained and are shown in Figure 4-11(a), (b), (c), (d), (e), and (f). A_0 is the least significant bit and each frequency response plot corresponds to one of the control bits on. It was observed that the output of the programmable attenuator is harmonically distorted beginning at 35 MHz with A_0 on and beginning at 40 MHz with A_1 on. No distortions were observed with other bit settings. The attenuator output was monitored on a spectrum analyser (Spectrum Analyser composed of a HP 85536 spectrum analyser RF section, a HP 8552A spectrum analyser IF section and a HP 140 B oscilloscope) to quantify the harmonic distortion. Table 4-3 shows the attenuation of the harmonics with frequency up to the fifth harmonic with the different bit settings of the attenuator. On Table 4-3 (a) with bit A_0 on, from 35 MHz onwards, a minimal

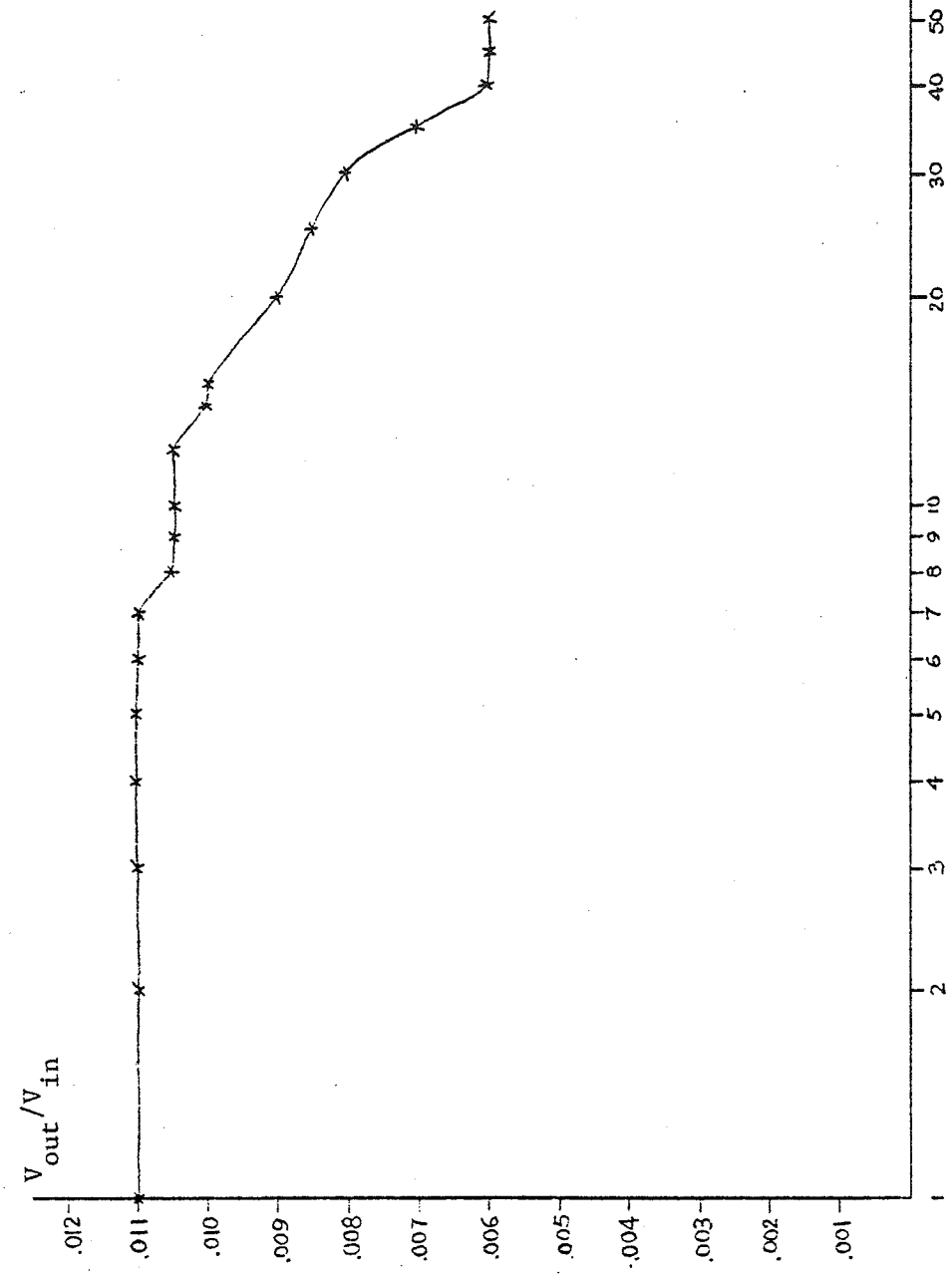


Figure 4-11(a): Frequency Response of Programmable Attenuator With Bit A_0 On

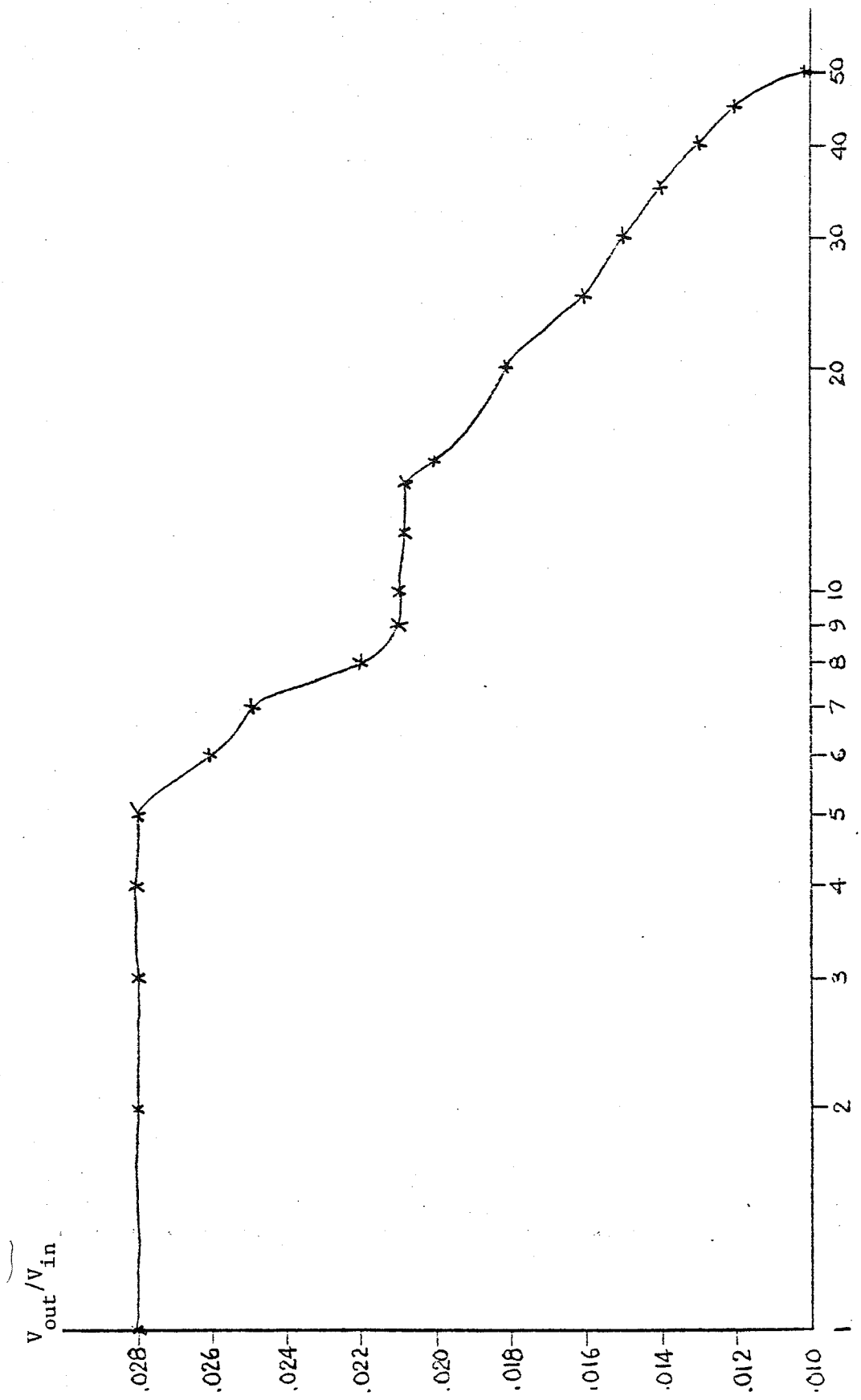


Figure 4-11(b): Frequency Response of Programmable Attenuator With Bit A_1 On

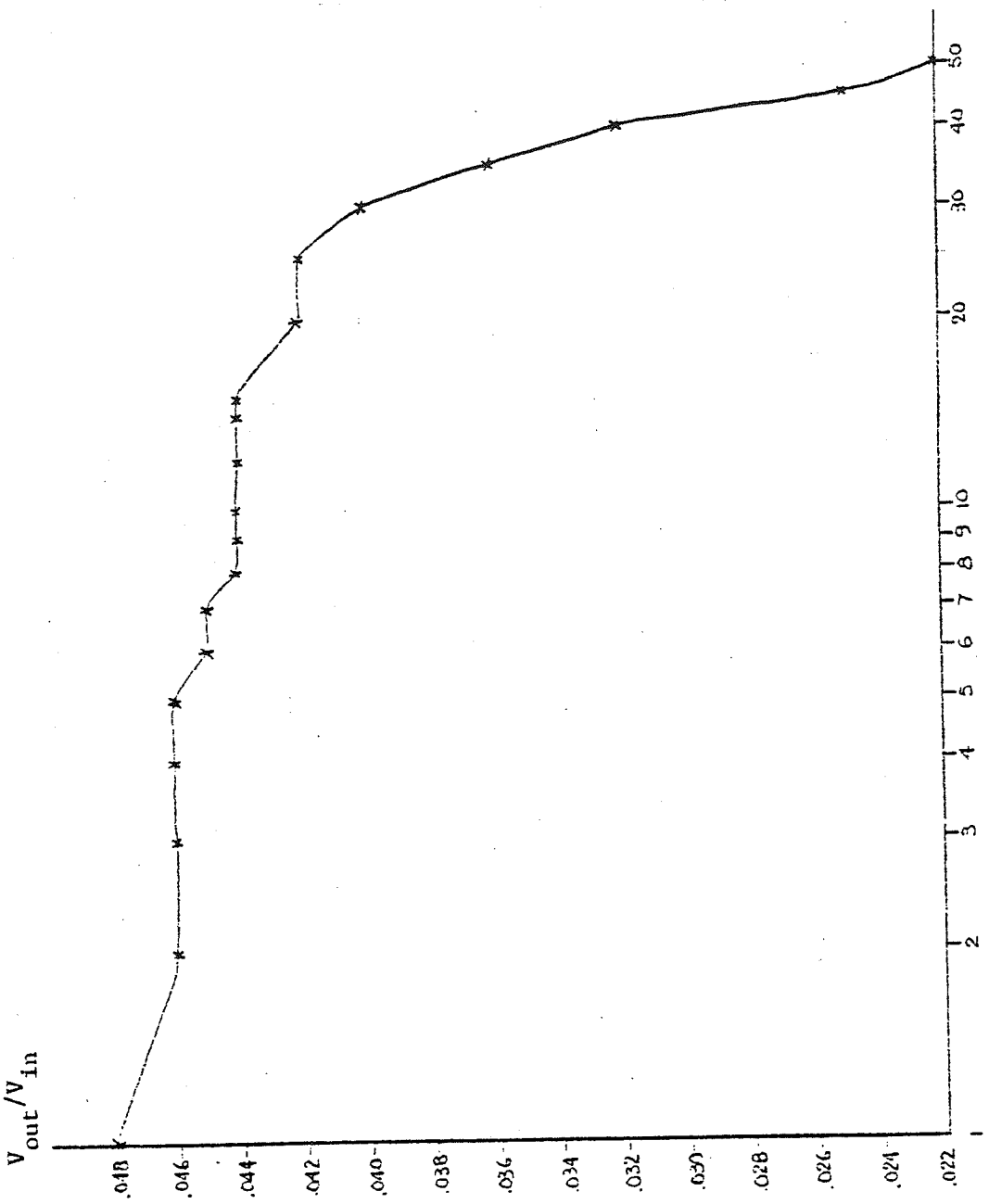


Figure 4-11(c): Frequency Response of Programmable Attenuator With Bit A_2 On

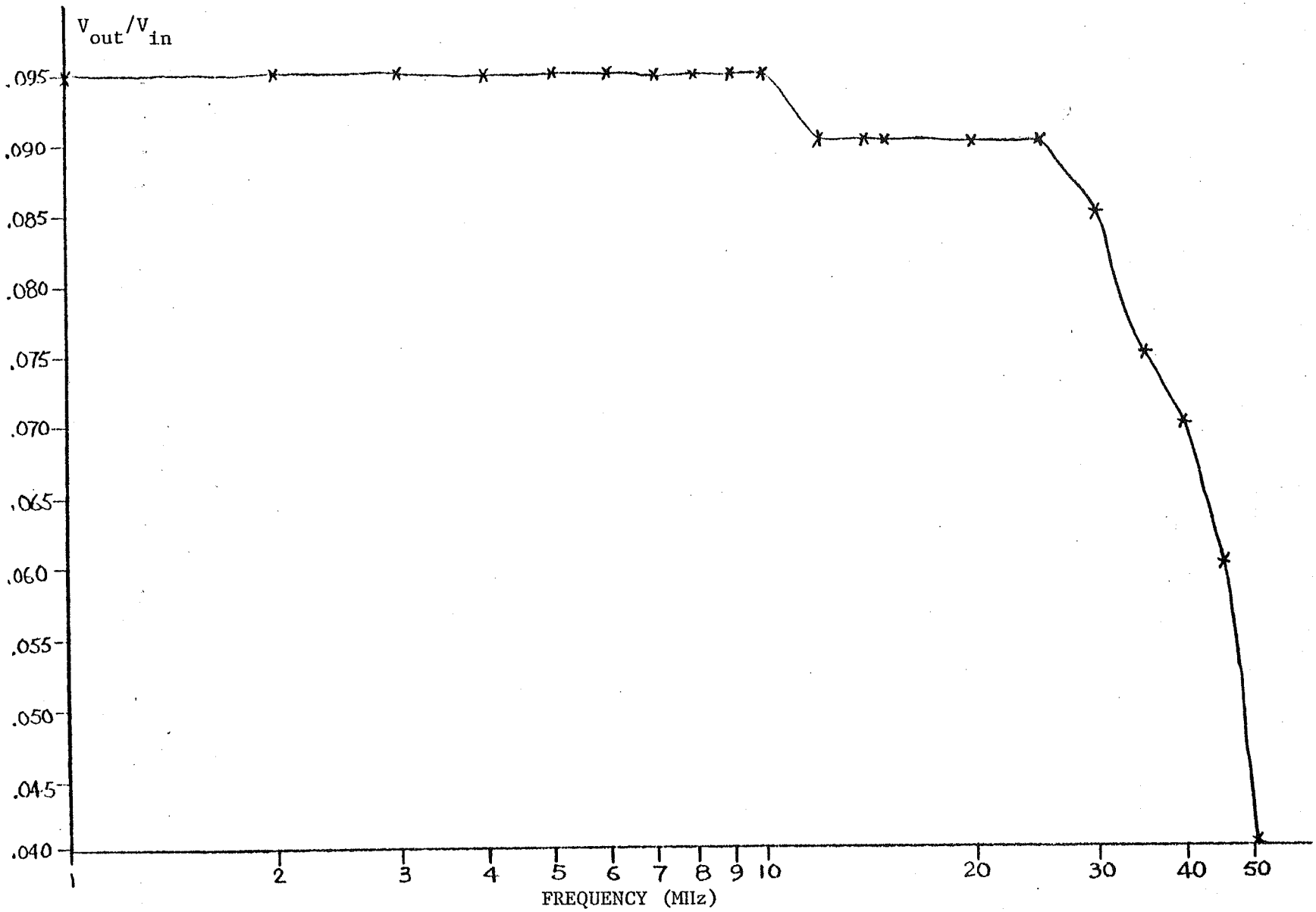


Figure 4-11(d): Frequency Response of Programmable Attenuator With Bit A_3 On

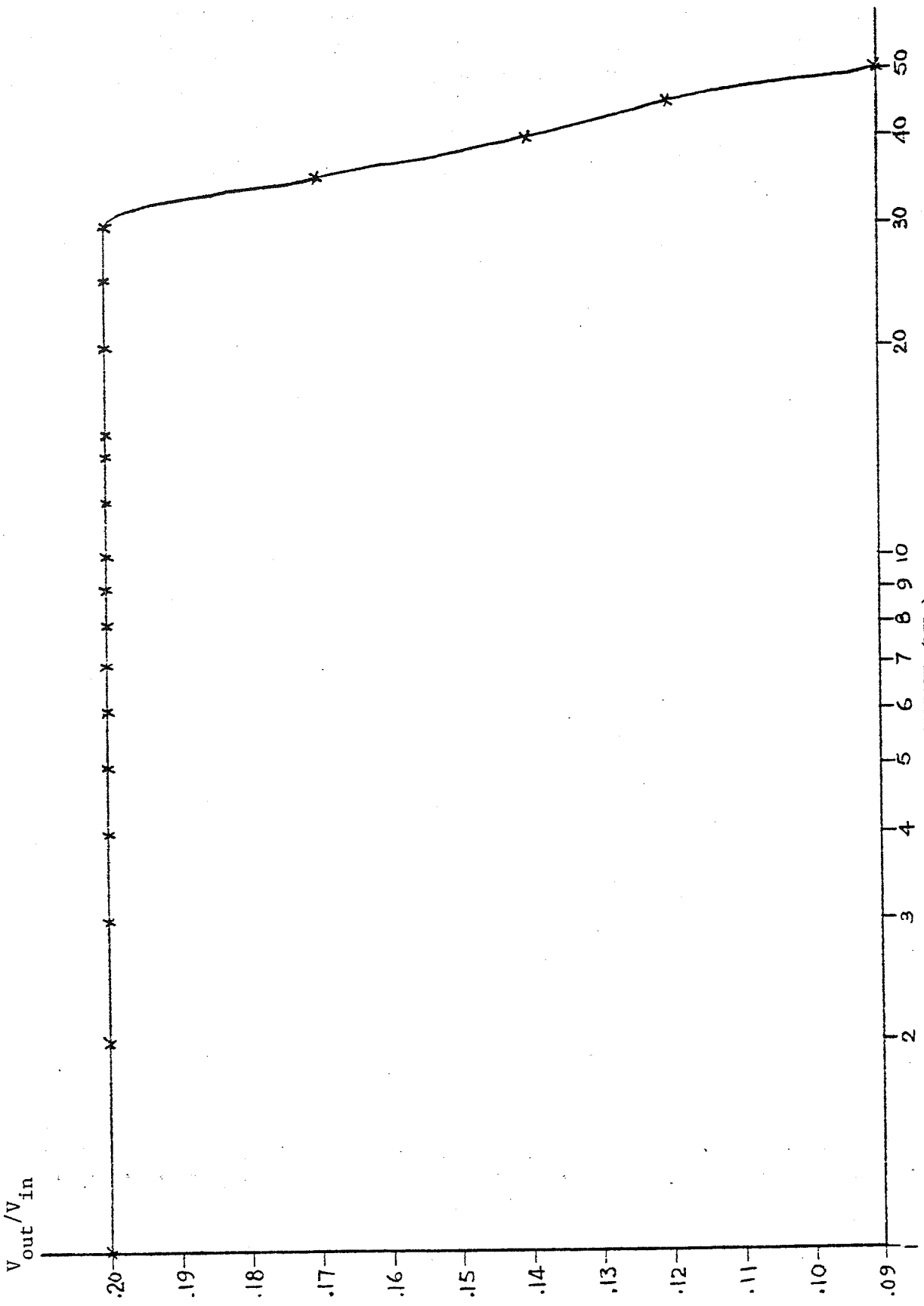


Figure 4-11(e): Frequency Response of Programmable Attenuator With Bit A_4 On

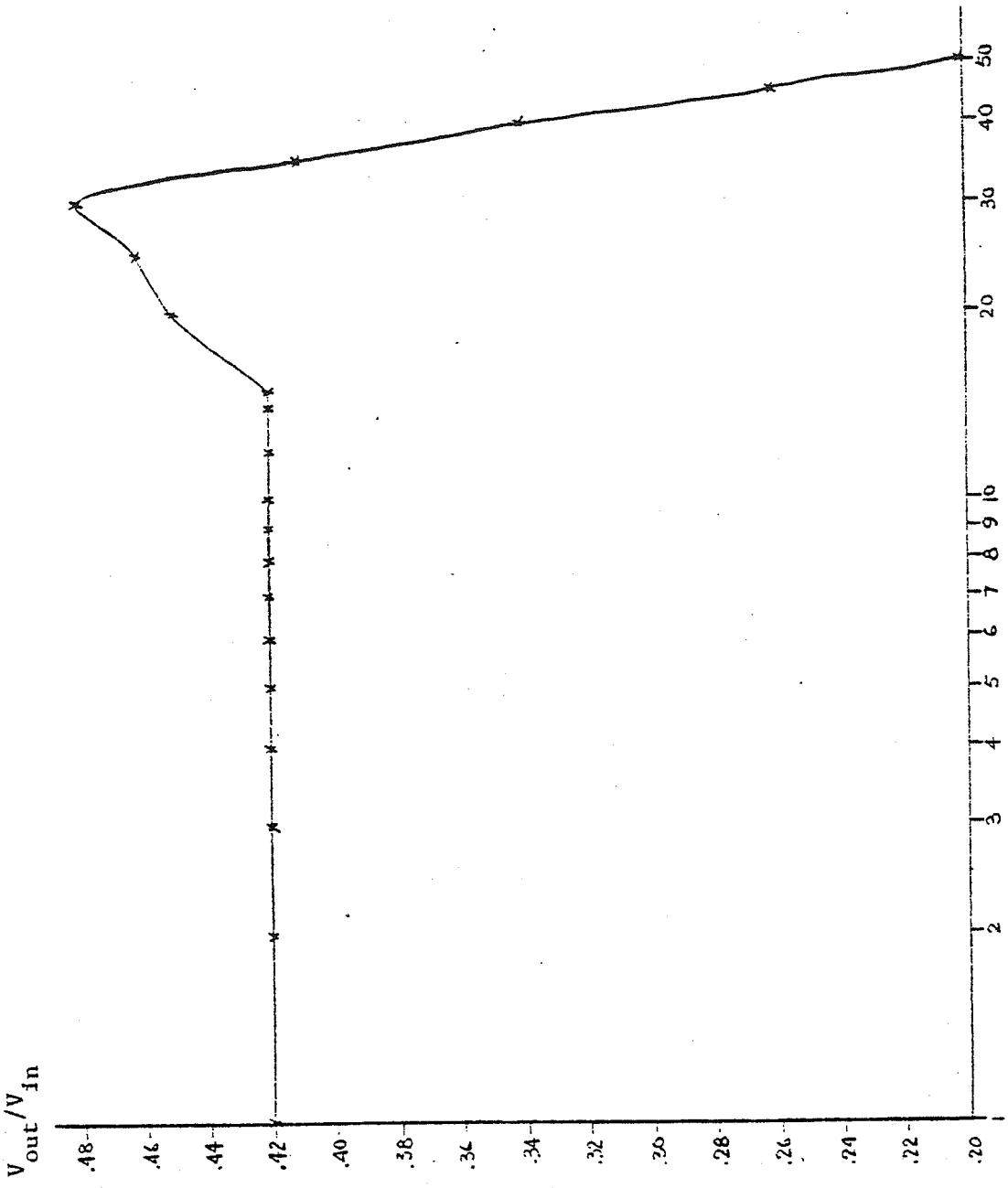


Figure 4-11(f): Frequency Response of Programmable Attenuator With Bit A_5 On

Table 4-3(a): Harmonic Levels With A_o On

(MHz)	(dB relative to fundamental)			
FREQ(fc)	2 fc	3 fc	4 fc	5 fc
1	- 47	*	*	*
2	- 50	*	*	*
3	- 50	*	*	*
4	- 47	*	*	*
5	- 50	- 50	*	*
6	- 50	- 50	*	*
7	- 50	- 48	*	*
8	- 50	- 47	*	*
9	- 50	- 45	*	*
10	- 50	- 45	*	*
12	- 50	- 44	*	*
14	- 48	- 40	*	*
15	- 50	- 40	*	*
20	- 43	- 38	*	- 52
25	- 43	- 40	*	- 50
30	- 38	- 35	*	*
35	- 40	- 29	+	+
40	- 35	- 25	+	+
45	- 33	*	+	+
50	- 31	*	+	+

* = less than - 50 dB
+ = exceed frequency range of spectrum analyser

Table 4-3(b): Harmonic Levels With A_1 On

(MHz)	(dB relative to fundamental)			
FREQ(fc)	2 fc	3 fc	4 fc	5 fc
1	- 50	*	*	*
2	- 50	*	*	*
3	- 50	*	*	*
4	- 50	*	*	*
5	- 50	- 54	*	*
6	- 54	- 54	*	*
7	- 54	- 52	*	*
8	- 54	- 50	*	*
9	- 52	- 50	*	*
10	- 50	- 46	*	*
12	- 46	- 44	*	*
14	- 47	- 44	*	*
15	- 45	- 43	*	*
20	- 45	- 46	*	*
25	- 46	- 46	*	*
30	- 38	- 34	*	*
35	- 50	- 36	+	+
40	- 44	- 30	+	+
45	- 40	*	+	+
50	- 36	*	+	+

* = less than - 50 dB
+ = exceed frequency range of spectrum analyser

Table 4-3(c): Harmonic Levels with A_2 On

(MHz)	(dB relative to fundamental)			
FREQ(fc)	2 fc	3 fc	4 fc	5 fc
1	- 45	- 52	x	x
2	- 50	x	x	x
3	- 54	- 57	x	x
4	- 57	- 60	x	x
5	- 55	x	x	x
6	- 55	- 60	x	x
7	- 54	- 60	x	x
8	- 54	- 55	x	x
9	- 52	- 52	x	x
10	- 50	- 50	x	x
12	- 47	- 47	x	x
14	- 46	- 45	x	x
15	- 45	- 43	x	x
20	- 45	- 50	x	x
25	- 46	- 54	x	x
30	- 50	- 52	x	x
35	- 52	- 42	+	+
40	- 53	- 37	+	+
45	- 46	x	+	+
50	- 42	x	+	+

x = less than - 60 dB
+ = exceed frequency range of spectrum analyser

Table 4-3(d): Harmonic Levels with A_3 On

(MHz)	(dB relative to fundamental)			
FREQ(fc)	2 fc	3 fc	4 fc	5 fc
1	- 40	- 42	-	- 60
2	- 45	- 53	-	- 60
3	- 52	- 52	-	- 60
4	- 52	- 52	-	- 62
5	- 52	- 51	-	- 60
6	- 54	- 52	-	- 60
7	- 53	- 51	-	- 62
8	- 51	- 50	-	- 62
9	- 50	- 50	-	- 64
10	- 46	- 49	- 65	- 64
12	- 45	- 46	- 65	- 65
14	- 44	- 45	-	-
15	- 44	- 44	-	-
20	- 44	- 52	-	-
25	- 45	- 51	-	-
30	- 44	- 50	-	-
35	- 47	- 44	+	+
40	- 54	- 42	+	+
45	- 52	-	+	+
50	- 50	-	+	+

- = less than - 65 dB
+ = exceed frequency range of spectrum analyser

Table 4-3(e): Harmonic Levels with A_4 On

(MHz)	(dB relative to fundamental)			
FREQ(fc)	2 fc	3 fc	4 fc	5 fc
1	- 29	- 19	- 50	- 44
2	- 34	- 29	- 60	- 50
3	- 41	- 32	- 60	- 50
4	- 41	- 33	- 60	- 50
5	- 40	- 36	- 60	- 48
6	- 41	- 38	- 60	- 48
7	- 42	- 38	- 58	- 50
8	- 41	- 38	- 58	- 49
9	- 41	- 36	- 57	- 48
10	- 40	- 35	- 56	- 48
12	- 40	- 33	- 56	- 52
14	- 40	- 34	- 58	- 54
15	- 41	- 35	- 60	- 55
20	- 42	- 37	- 66	- 66
25	- 40	- 34	- 68	Δ
30	- 42	- 31	- 60	Δ
35	- 42	- 32	+	+
40	- 46	- 34	+	+
45	- 47	Δ	+	+
50	- 46	Δ	+	+

Δ = less than - 68 dB
+ = exceed frequency range of spectrum analyser

Table 4-3(f): Harmonic Levels with A_5 On

(MHz)	dB			
FREQ(fc)	2 fc	3 fc	4 fc	5 fc
1	- 32	- 24	- 54	- 42
2	- 38	- 37	- 60	- 44
3	- 46	- 36	- 60	- 44
4	- 45	- 36	- 60	- 43
5	- 46	- 35	- 58	- 42
6	- 46	- 33	- 56	- 42
7	- 45	- 33	- 55	- 43
8	- 45	- 32	- 55	- 43
9	- 44	- 32	- 54	- 44
10	- 44	- 32	- 54	- 44
12	- 44	- 33	- 55	- 46
14	- 42	- 35	- 57	- 46
15	- 41	- 35	- 58	- 47
20	- 37	- 32	- 65	- 50
25	- 35	- 30	- 65	/
30	- 35	- 30	- 54	/
35	- 35	- 30	+	+
40	- 35	- 28	+	+
45	- 38	/	+	+
50	- 38	/	+	+

/ = less than -67 dB
+ = exceed frequency range of spectrum analyser

attenuation of 25 dB was observed with the third harmonic at 40 MHz. It is suspected that there might be higher harmonics with even less attenuation which accounts for the observed distortion. On Table 4-3(b) with A_1 on; from 40 MHz onwards, a minimal attenuation of 30 dB was observed to occur at 40 MHz with the third harmonic. As in the case with A_0 on, higher harmonics with even less attenuation might account for the observed distortion. The maximum operation frequency of the attenuator is therefore 30 MHz.

4.1.6 Buffer Amplifiers

4.1.6.1 Device Description

National's LH 0063CK buffer amplifier is used. These devices have a 100 MHz bandwidth, 4000 V/μs slew rate and a drive capability of ± 250 mA into 50 Ω loads. This device is used at the output of the double balanced mixer and at the output of the receive transducer before the HP 461 A amplifier. At the double balanced mixer output, the input to the buffer amplifier is terminated at 50 Ω and the amplifier isolates the double balanced mixer output from the changing input impedance of the ladder network of the programmable attenuator. At the receive transducer output, the buffer amplifier's FET input provides a high input impedance (10^{10} Ω) to the transducer and prevents the transducer output signal from being loaded down by the 50 Ω input impedance of the HP 461 A amplifier should the buffer amplifier be omitted. There is also a buffer amplifier to the input of the TRW video A/D for protection. Since this buffer amplifier, the TRW video A/D and the parallel memory buffer are not implemented in the data acquisition system, this buffer amplifier will not be discussed.

4.1.6.2 Performance Evaluation

The buffer amplifiers were tested by terminating the amplifier input with a 50 Ω load and driving the amplifier input with a 1 V_{o-p} signal from the HP 8660B synthesizer. The output of the amplifier is terminated with a 50 Ω load and monitored on a scope. Figure 4-12 shows the frequency response of the buffer amplifiers.

4.1.7 Power Amplifier

4.1.7.1 Device Description

This instrument amplifies the coherent tone-burst signal at the output of the programmable attenuator in order to drive the transmit transducer to produce ultrasound signal. The ENI model 310L RF power amplifier is used. According to the manufacturer this amplifier has a gain of 50 dB from 250 kHz to 110 MHz into a 50 Ω load and an input impedance of 50 Ω with 1 V maximum input.

4.1.8 Clipper

4.1.8.1 Device Description

This is a signal detection circuit to be used in time-of-flight (TOF) measurement. This circuit has two identical input channels and two TTL output channels. Each input channel detects both a positive going and a negative going signal and generates a falling edge as output. To measure (TOF), the clipper detects any signal at the programmable attenuator output and generates a single falling edge at its A output. This falling edge drives channel A of the HP 5328A universal counter and starts the counter. The ultrasound signal is received by the receive transducer and amplified by the HP 461A amplifier. The amplified received signal is detected by the clipper at the other input channel and generates

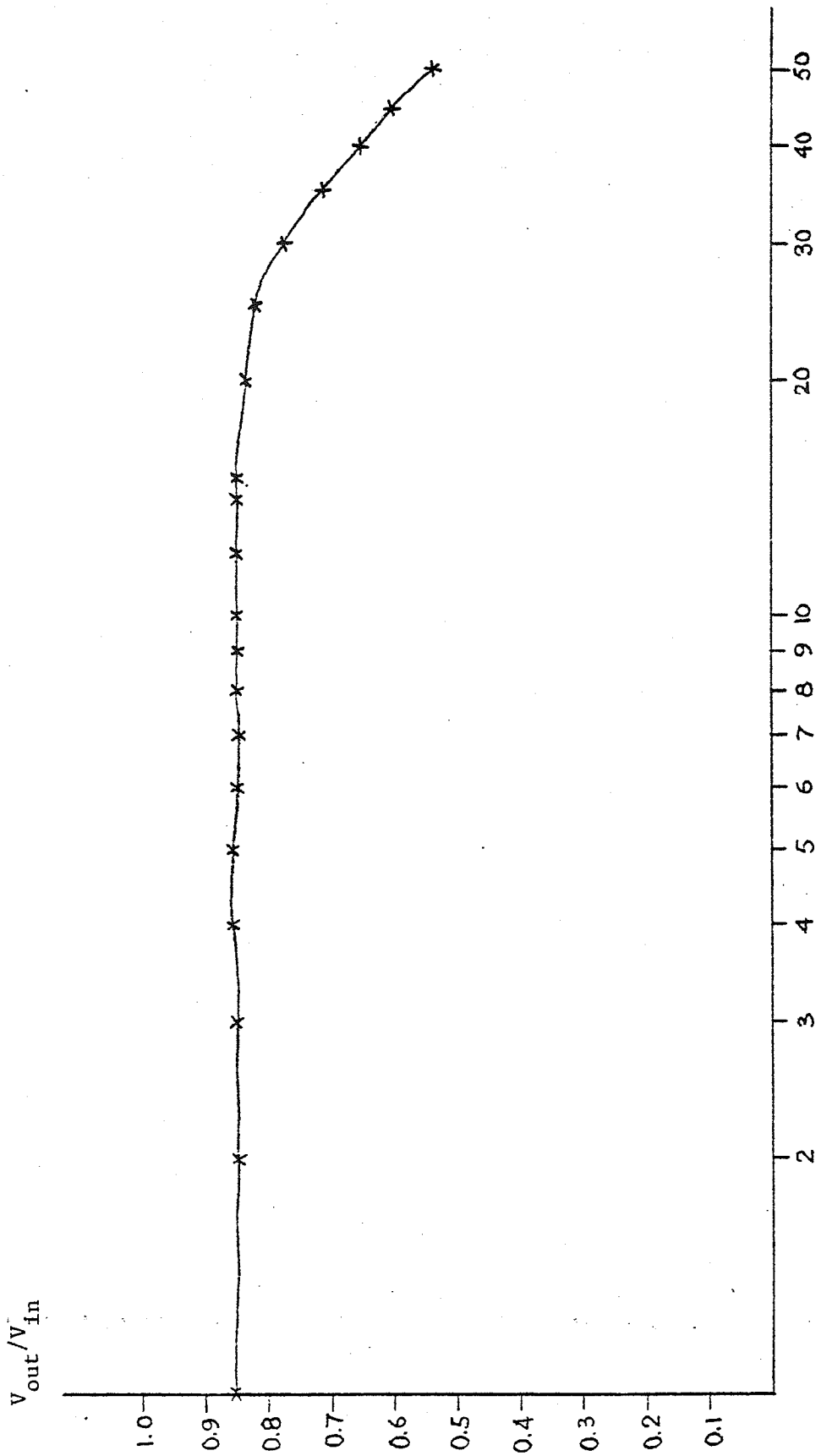


Figure 4-12: Frequency Response of Buffer Amplifier

a single falling edge at its B output. This falling edge trigger the B input channel of the HP 5328 A universal counter and stops the counter. Due to the utilization of an S-R latch at the output section of the clipper circuit, only a single falling edge will be generated to each of the counter inputs upon detection of the first signal edge. This property is essential as erronous counting will result should multiple trigger is experienced at the B input channel of the counter when stopping the counter.

4.1.8.2 Circuit Description

The clipper circuit is located on Board A4 (Figure A-7 of Appendix A). This circuit has two identical channels (A and B) and each channel has the capability of detecting a positive going signal or a negative going signal. On each channel, signal detection is accomplished by two voltage comparators. One comparator switches upon seeing a positive going signal and the other comparator switches on a negative going signal. The ECL voltage comparator Advanced Microdivce's AM 687 (IC's(DX) and (BX)) is used.

On channel A, the non-inverting inputs (pins 8 and 9 of IC(DX)) of the two comparators are biased to + 10 mV and - 10 mV respectively to eliminate any erronous switching due to noise. Pin 2 of IC(DX) will go "high" when a positive going signal go above + 10 mV and pin 16 of IC(DX) will go "high" when a negative going signal go below - 10 mV. The ECL outputs of IC(DX) are transformed into TTL level by IC(CX). The transformed output at pins 5 and 12 of IC(CX) are then "NORed" by IC(CY). Pin 4 of IC(CY) drives the $\overline{S}$ input (pin 4 of IC(BY)) of the $\overline{SR}$ latch implemented by IC(BY). The first switching at pin 4 of IC(CY) from "high" to "low" will set the Q output (pin 6 of IC(BY)) of the $\overline{SR}$ latch to "high." With no signal at A_{in}, pins 5 and 12 of IC(CX) will stay at "low" and pin 4 of IC(CY) stays at

"high."

Channel B has the same circuit at A, except the non-inverting inputs of the two comparators are biased to +/ - 50 mV. Any signal at A_{in} will set the $\overline{SR}$ latch and any signal at B_{in} will reset the $\overline{SR}$ latch. The Q and $\overline{Q}$ outputs (pins 6 and 12 respectively of IC(BY)) are inverted by the 50 Ω line driver IC(AY). Channel A and B of the HP 5328A counter must therfore be set to negative-slope triggered. The inputs to the comparators are AC coupled and protected by the series diodes.

The latch is reset manually by the clipper reset switch on the system front panel, reset by an automatic reset pulse 105 μs after channel A "fired," or reset by a pulse generated by the computer. During automatic reset, a reset pulse is triggered by the Q output of the $\overline{SR}$ latch. The purpose of the atuomatic reset is to eliminate the trouble of resetting the clipper should the received ultrasound signal is too weak to reset the clipper. The automatic reset feature can be disabled by setting bit 1 of the clipper control status register CLIPCSR to logic 0. The user can thus disable this automatic reset feature should there be any possibility of the time-of-flight of the ultrasound signal exceeds 105 μs.

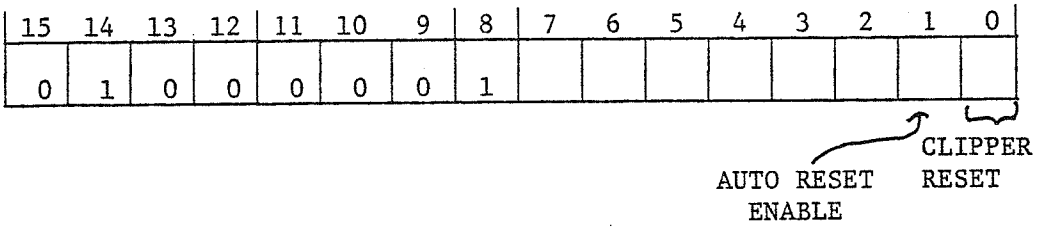
4.1.8.3 Controller (DEVICE 4)

4.1.8.3.1 Control Word Format and Programming Guide

Apart from the atuomatic reset circuitry, the clipper can be reset by writing a "1" into bit 0 of CLIPCSR (address = 000). Every time a "1" is written into bit 0 of the register, a 1 μs pulse is generated to reset the clipper. This "controlled reset pulse" is actually "ORed" with the output of automatic reset circuitry. The automatic reset is disabled by writing a 0 into bit 1 of CLIPCSR. To provide more flexibility to the user, the states of the

outputs of channels A and B of the clipper can be read by reading CLIPBUF. Figure 4-13 gives the formats of the control words.

CLIPCSR (write only)



CLIPBUF (read only)

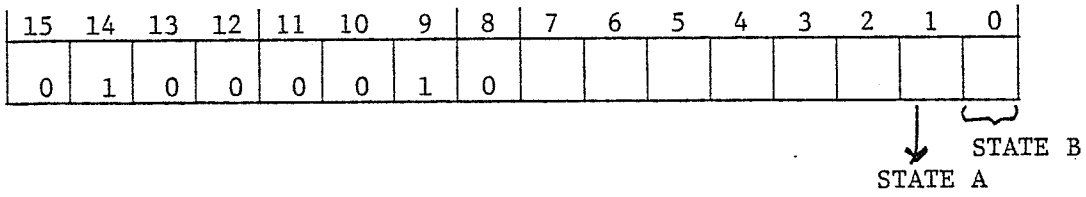


Figure 4-13: Control Word Formats for the Clipper

4.1.8.3.2. Controller Circuit Description (Board D8)

The controller circuit is located on Board D8 (Figure A-8 of Appendix A). IC(AV) acts as a demultiplexor routing the 1 µs DOPDA to its YO output at pin 15 when DEVICE 4 and CLIPSCSR are addressed and the write mode is used. Since YO has an inverted output, the inverted pulse is reinverted by IC(AW) at pin 4. Should a "1" be written into bit 0 of CLIPCSR, the 1 µs pulse is gated to pin 6 of IC(BW) and routed to pin 3 of IC(CV).

The output state of channel A of the clipper (STATE A) triggers a 105 µs one-shot (IC(CW)). This is the timing pulse which triggers a 1 µs reset pulse at its falling edge. This automatic reset pulse is gated by IC(DZ) and ORed and

inverted (or NORed) with the controlled reset pulse from the computer and routed to the clipper board to reset the clipper. This automatic reset feature is enabled by writing a 1 into bit 1 of CLIPCSR and setting pin 9 of IC(DX) to "high."

When CLIPBUF is addressed and during read mode, IC(BV) acts as a decorder and activates the tri-state driver IC(DY) to enable the states of output channels A and B (STATE A and STATE B respectively) of the clipper to be read in by the computer.

4.1.8.4 Performance Evaluation

The Am 687 voltage comparators output a square wave with 3.5 ns fall time and 5 ns rise time at 50 MHz. Figure 4-14 gives a scope trace of the comparator output at 50 MHz after being translated to TTL level. The clipper circuit was tested by performing time-of-flight measurements with the clipper outputs driving the HP 5328A universal counter. A description of the experiment and results are given in Chapter 5 System Evaluation.

4.1.9 HP 5328A Universal Counter

4.1.9.1 Device Description

This instrument is used for measuring the time-of-flight (TOF) of the ultrasound signal through the tissue-under-test. The time interval averaging mode of the instrument is used to achieve a resolution of 2 ns and requires averaging of 100 intervals. The 5328A function, resolution, remote/local, reset and Option 041 input module are remotely programmable.

4.1.9.2 Interface Specifications

Control signals are applied through a 24 pin microribbon connector labeled

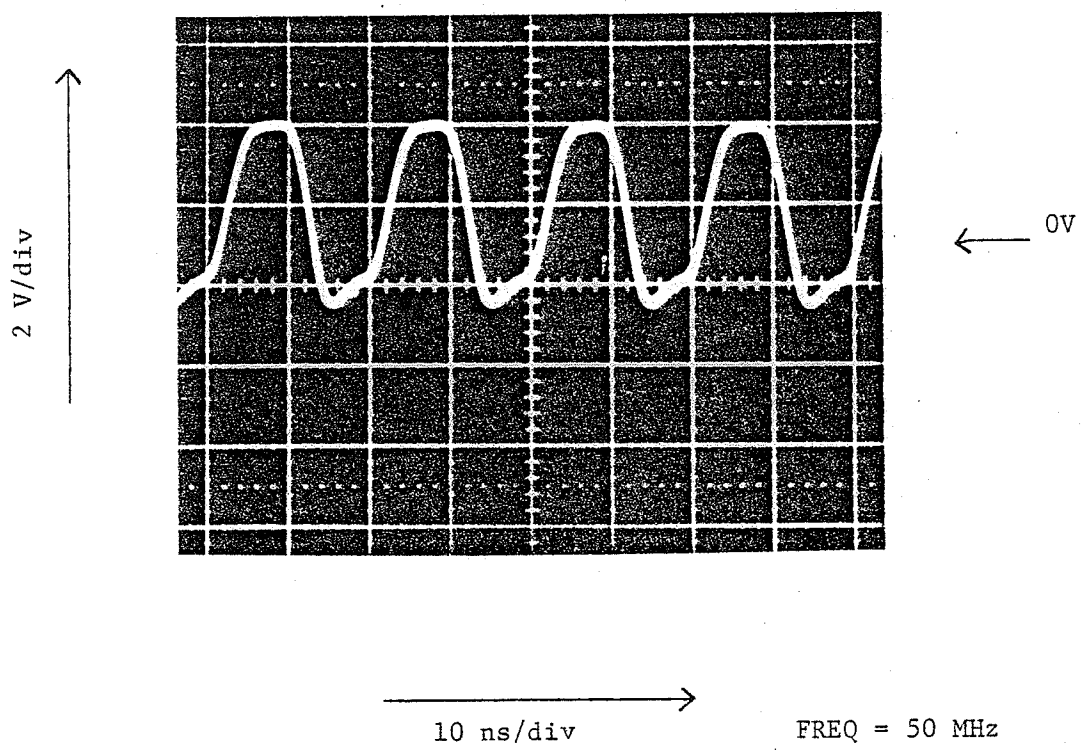


Figure 4-14: Voltage Comparator Outputs of the Clipper Circuit

REMOTE PROGRAMMING and BCD outputs of the counter can be read from a 50 pin blue ribbon connector labeled DIGITAL RECORDER. Both connectors can be found at the back of the instrument. Programming details and control signal descriptions are not discussed here and the user must reference (5) for details.

4.1.9.3 Controller (Device 3)

4.1.9.3.1 Control Word Format and Programming Guide

When programming this instrument, the user should always refer to reference (5) for the control bit definitions and programming details. Figure 4-15 gives the control word formats for programming the counter. The read-only recorder buffer registers RECORDER-BUF-A and RECORDER-BUF-B are 16 bits long.

4.1.9.3.2 Controller Circuit Description (Device 3)

The controller circuit is located on Board D7 (Figure A-9 of Appendix A). During write mode the demultiplexor IC(AV) routes DOPDA as a strobing pulse to the various latches/flip-flops. The select inputs OBIT 9, OBIT 10, and OBIT 11 to IC(AC) are the register address bits. IC(DX) latches bits 0 to 6 of FTB-BUF, IC(BX) latches bits 0 to 4 of 041A-BUF, IC's(CX) and (CY) latches bits 0 to 3 of 041-CSR and IC(BW) latches bits 0 and 1 of RECORDER-CSR.

During read mode, IC(AT) decodes the "read" condition and enables the corresponding tri-state drivers of the addressed register. The four drivers in IC(CW) routes bits 0 and 3 of 041-CSR to the 16 bit input of DIO 1 when enabled while the remaining two drivers of IC(CW) and one driver of IC(BZ) routes bits 0 to 2 of RECORDER-CSR to the 16 bit input when enabled. RECORDER-BUF-A, RECORDER-BUF-B and RECORDER-BUF-C, which holds the ten BCD digit outputs of the counter, are read by enabling the tri-state drivers of IC's(AX), (BZ), (AY), (CZ), (DZ), (DY),

FTB-BUF (function and time base)
Addr = 000 (write only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	1								

$\overline{IBA}$ $\overline{TBB}$ $\overline{TBC}$ $\overline{FA}$ $\overline{FB}$ $\overline{FC}$ $\overline{FD}$

Time Base Function

041B-BUF (041 input section, channel B programmings)
Addr = 001 (wirte only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	1								

Invert or Normal; Atten Slope; Coupling; Imp

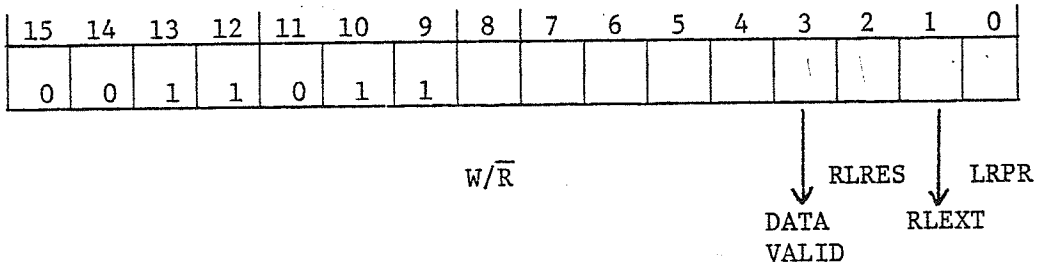
041A-BUF (041 input section, channel A programming)
Addr = 010 (write only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	1	0	1								

Sep-Com; Atten; Slope; Coupling; Imp

Figure 4-15(a): Control Word Format for HP5328A Counter (DEVICE 3)

041-CSR (041 input section control status)
Addr = 011 (read/write)



RECORDER-CSR (recorder control status)
Addr = 100 (read/write)

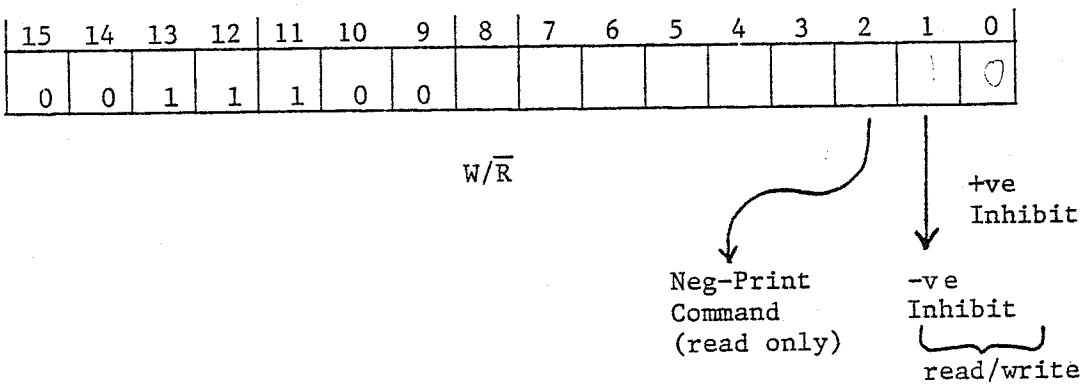
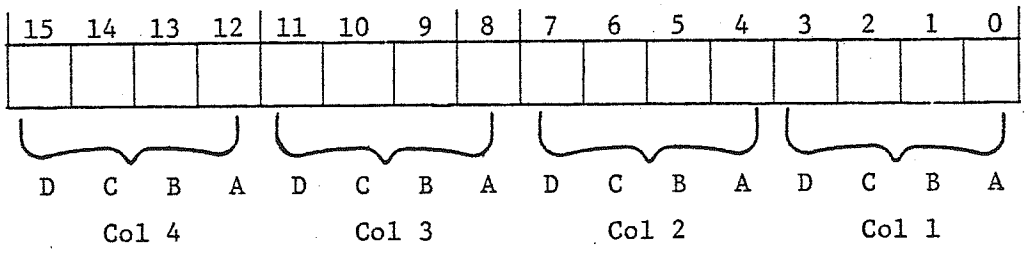
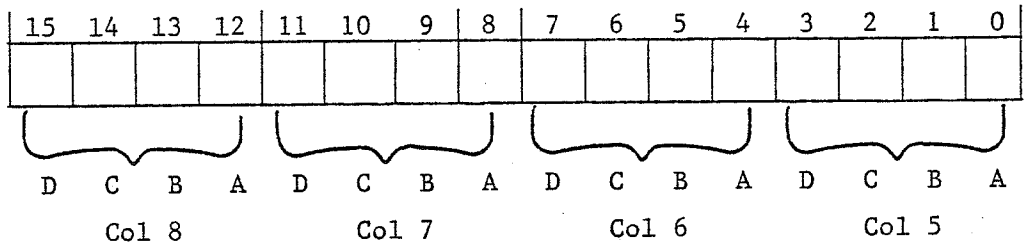


Figure 4-15(b): Control Word Format For HP 5328A Counter (DEVICE 3)

RECORDER-BUF-A
Addr = 101 (read only)



RECORDER-BUF-B
Addr = 110 (read only)



RECORDER-BUF-C
Addr = 111 (read only)

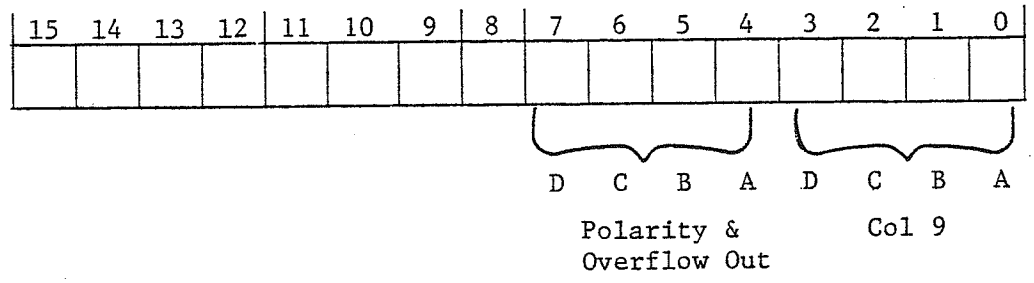


Figure 4-15(c): Control Word Format for HP 5328A Counter (DEVICE 3)

(DZ), and (DW).

4.1.10 HP 461A Amplifier

4.1.10.1 Device Description

This amplifier amplifies the received ultrasound signal to trigger channel B of the clipper circuit.

As stated in the manuel of this device, this amplifier has a frequency response of 1 kHz to 150 MHz into a 50 Ω resistive load. It has a 50 Ω input impedance and 1 volt rms or 2 volts p-p pluse maximum input. Maximum output is 0.5 volt rms into 50 Ω resistive load. For more detail specifications of this amplifier, the user should consult reference (7).

4.1.11 20 MHz Low Pass Filter

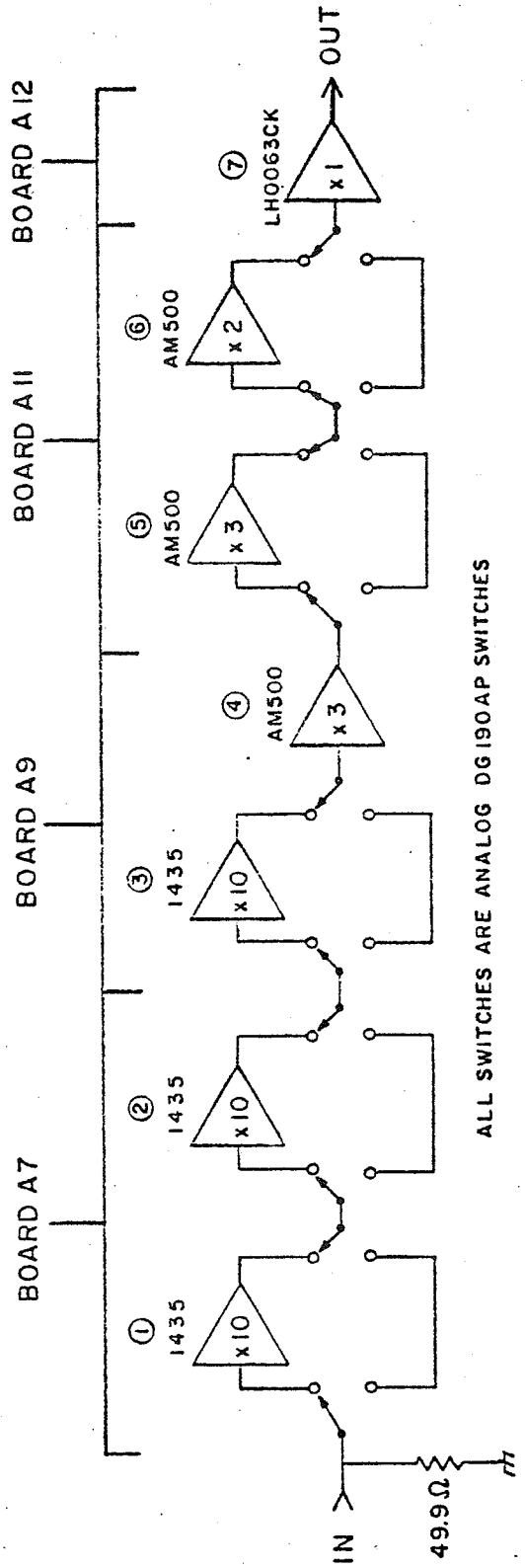
4.1.11.1 Device Description

This device is intended to eliminate unwanted high frequency noise when a tone-burst signal is transmitted. This filter is by-passsed during the broad band pulse mode. It is a nine element filter made by CIRQTEL (part number: LR9-20CD). It has 50 Ω input/output impedance and an attenuation of greater than 60 dB at 36 MHz as stated by CIRQTEL. With a 1 V_{o-p} signal at the filter input and output monitored on a scope with 50 Ω termination, the observed attenuation is -0.54 dB at 10 MHz, -1.31 dB at 20 MHz, -24.44 dB at 25 MHz, and -50.46 dB at 36 MHz.

4.1.12 Programmable Gain Amplifier

4.1.12.1 Device Description

The programmable gain amplifier has a total of seven stages with a total gain of 85 dB. A block diagram of the amplifier is given in Figure 4-16. There are



* ALL SWITCHES ARE SILICONIX DG 190AP ANALOG SWITCHES

Figure 4-16: Programmable Gain Amplifier Block Diagram

three X10 stages implemented by the Teledyne Philbrick's 1435 (1 GHz gain bandwidth) operational amplifier, two X3 stages and one X2 stage implemented by Datel's AM 500 (100 MHz gain bandwidth) operational amplifier and X1 stage implemented by National's LH 0063CK buffer amplifier (100 MHz). Different gain settings can be obtained by either "tunning-in" or by-passing the different fixed gain amplifier stages. The switching in and out of these amplifier stages are achieved by analog switches (DG 190AP by Siliconix). As can be seen from Figure 4-16, the first X3 stage cannot be by-passed. This is due to the fact that the analog switches have an ON resistance of 30 Ω and this fixed X3 stage is used to isolate the three X10 stages from the later stages in order to reduce the gain variation as a result of the 30 Ω ON resistance being added to the input resister at the later stages should this first X3 stage be made programmable. The X1 stage at the output section gives the programmable gain amplifier a 50 Ω drive capability.

An earlier design of the amplifier based on Figure 4-17 was proved to be unsuccessful. The initial design physiology was to put several gain setting on a single stage amplifier and several of these variable gain stages were patched together to form the programmable gain amplifier. In Figure 4-17, different gains will be obtained as a result of changing the effective resistance from the inverting input to ground. However, due to the effective OFF capactance of the switches to ground (estimaged reactance of about 1.59 Ω at 5 MHz), drastic changes of gain with frequency was observed as a result of variations of the effective resistance with frequency from the inverting input to ground. This gain variation with frequency thus proves the original design not useable.

4.1.12.2 Circuit Description

The programmable gain amplifier stages are located on Boards A7, A9, A11, and

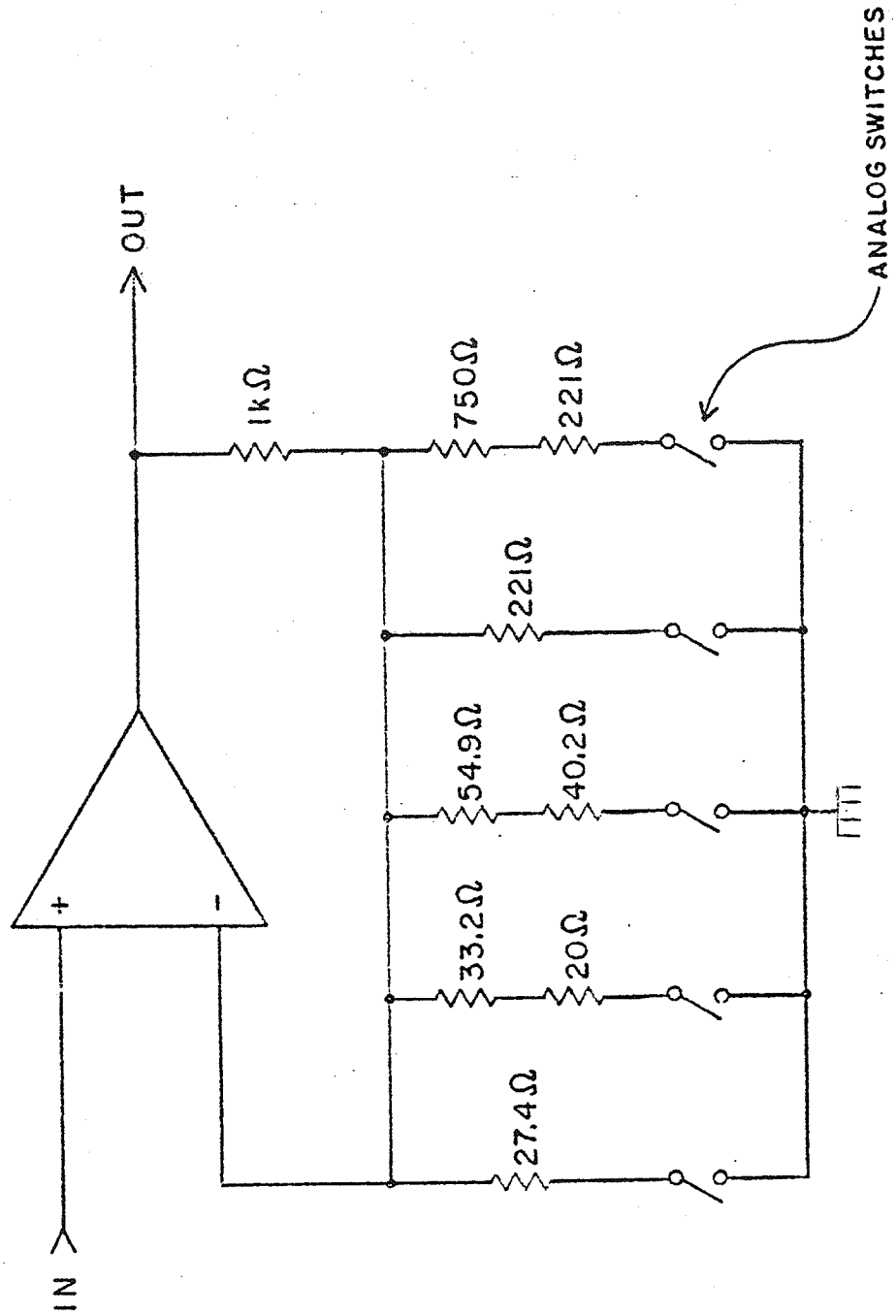


Figure 4-17: An Earlier Design of the Programmable Gain Amplifier

A 12 (Figure A-10 of Appendix A). Since some stages are identical only typical stages of X10, X3, X2, and X1 will be discussed and the user is assumed to be familiar with the specifications of the amplifier integrated circuits used.

4.1.12.2.1 Stages 1, 2, and 3, Gain = 10

The operational amplifier (Teledyne Philbrick 1435, gain bandwidth = 1 GHz) is connected as an inverting amplifier. The resister divider at the output allows 1/10 of the output signal to be fed back to the virtual ground through the 1 kΩ resistor. The input 909 Ω resistor to the virtual ground together with two switch ON resistance (30 Ω per switch) makes an effective input resistance of about 1 kΩ to the virtual ground. A gain of ten at the amplifier output is thus achieved. This configuration of feeding back 1/10 of the output signal to provide a gain of ten is essential to make all resistor values not to exceed 1 kΩ. Each of these X10 stage is driving a 300 pF capacitor in series with an approximate resistance of 1 kΩ to the next stage. This 300 pF and 1 kΩ pair acts as a high-pass filter with a cut-off at approximately 530 kHz, thus blocking off any possible off-set from the amplifier and any possible unwanted low-frequency noise. The analog switches accepts TTL level control signals and a logical 1 will cause the double-pole-double-throw switch to connect to the fixed gain amplifier stage. The amplifier stage is by-passed at a logical 0 input.

4.1.12.2.2 Stages 4 and 5, Gain = 3

The operational amplifier (Datel Am 500 gain bandwidth = 100 MHz) is connected as an inverting amplifier with a 3 kΩ feedback resistor and a 1 kΩ input resistor to the virtual ground. A gain of about three is achieved at the output. The output is AC coupled through a 300 pF capacitor to the next stage thus blocking off any

offset and possible low frequency noise. The double-pole-double-throw analog switch accepts TTL level control signals. This fixed gain amplifier stage is "tuned-in" at a logical 1 input and by-passed otherwise.

4.1.12.2.3 Stage 6, Gain = 2

This stage, as in stage 5, the Datel AM 500 is connected as an inverting amplifier with a 2 kΩ feedback resistor and a 1 kΩ input resistor thus giving a gain of about two. The output is also AC coupled through a 300 pF capacitor to eliminate offset and low frequency noise. A double-pole-double-throw analog switch is also used to switch in and out of this fixed gain amplifier. A logical 1 will cause this amplifier to be switched in.

4.1.12.2.4 Stage 7, Gain = 1

This is a buffer amplifier to provide a 50 Ω output drive at the output section of the amplifier chain. The circuit is similar to the buffer amplifier used at the output of the double balanced mixer and at the output of the receive transducer.

4.1.12.3 Controller (Device 5)

4.1.12.3.1 Control Word Format and Programming Guide

Since only stages 1, 2, 3, 5, and 6 are programmable, a single buffer register PAMP-BUF is used for programming the programmable gain amplifier. Figure 4-18 gives the control word format of PAMP-BUF. A logical 1 written in any of the bits 0 to 4 will switch in the corresponding stage. The analog switches used have a turn-on time of 150 ns and a turn-off time of 130 ns.

PAMP-BUF (read/write)
(addr = 000)

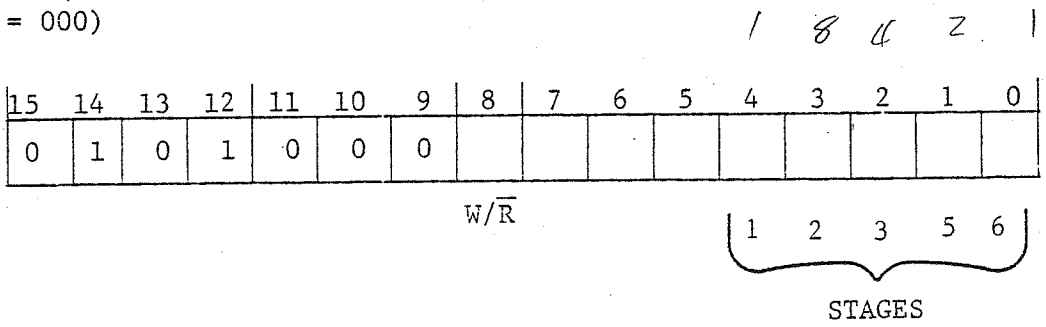


Figure 4-18: Control Word Format For The Programmable Gain Amplifier

4.1.12.3.2 Controller Circuit Description

The controller circuit is located on Board D8 (Figure A11 of Appendix A). During write mode, the demultiploxor IC(AX) routes the 1 μs DOPDA to pin 9 of IC(BY) as a strobing pulse. $\overline{\text{DEV 5}}$, which is a signal output as a result of decoding bits 12 to 15 of PAMP-BUF drives the enable inputs of IC(AX). IC(BY) latches bits 0 to 4 of PAMP-BUF.

During read mode, IC(BX) acts as a decoder, decoding the read condition and enables the tri-state drivers of IC(CY) if PAMP-BUF is addressed. IC(CY) drives the tri-state bus of the 16 bit input of DIO 1 and enables PAMP-BUF to be read.

4.1.12.4 Performance Evaluations

The programmable gain amplifier was tested by disconnecting stage 4 from stage 5. Frequency responses of different gain settings of stages 1, 2, 3, and 4 were obtained by feeding a signal from the snythesizer to the 49.9 Ω terminated input before stage 1 and monitoring the output of stage 4 by a scope probe. Frequency responses of different gain settings of stages 5, 6, and 7 were obtained by feeding a signal from the synthesizer to the input of the analog switch before stage 5 and with a 49.9 Ω termination. The output of stage 7 is terminated with

a 49.9 Ω load and monitored with a scope. Figure 4-19 (a), (b), (c), (d), (e), (f), (g), and (h) gives the different frequency response plots. Harmonic distortion was observed beginning at 20 MHz in Figure 4-19 (a) (gain = 3000) and beginning at 35 MHz in Figure 4-19 (b) (gain = 300). These distortions might be due to noise generated by the operational amplifiers and the distortion effects increases as the output signal starts to roll-off and the signal to noise ratio decreases. The noise level of stages 1, 2, 3, and 4 with different gain settings were investigated by removing the synthesizer signal from the terminated input before stage 1. The output of stage 4 was connected to a 950 Ω series resistor and routed to the 50 Ω input of a spectrum analyser. The 950 Ω series resistor is necessary due to the fact that the Datel AM 500 operational amplifier used in the implementation of stage 4 cannot drive a 50 Ω load. The loading of stage 4 due to the later stages is approximately 1 kΩ and the 950 Ω series resistor into the 50 Ω input impedance of the spectrum analyser would be close to the actual loading. The noise level due to different gain settings was measured by the spectrum analyser. Similarly, the signal to the input of the switch before stage 5 was removed and the input of the analog switch is terminated with a 49.9 Ω to ground. The output of stage 7 is connected directly to 50 Ω input of the spectrum analyser (stage 7 has 50 Ω drive capability). The noise level with different gain settings of stages 5, 6, and 7 were measured with the spectrum analyser. Table 4-4 gives a summary of the noise level measurements with the spectrum analyser. Noise level measurements were also performed by using a 250 MHz bandwidth oscilloscope. The output of stage 4 was monitored on a scope with a scope probe and without any signal at the terminated input before stage one. The output of stage 7 was also monitored on a scope with a 50 Ω termination and the inputs to the switch before stage 5 was terminated with a 50 Ω load. Table 4-5 shows the observed noise level with the scope.

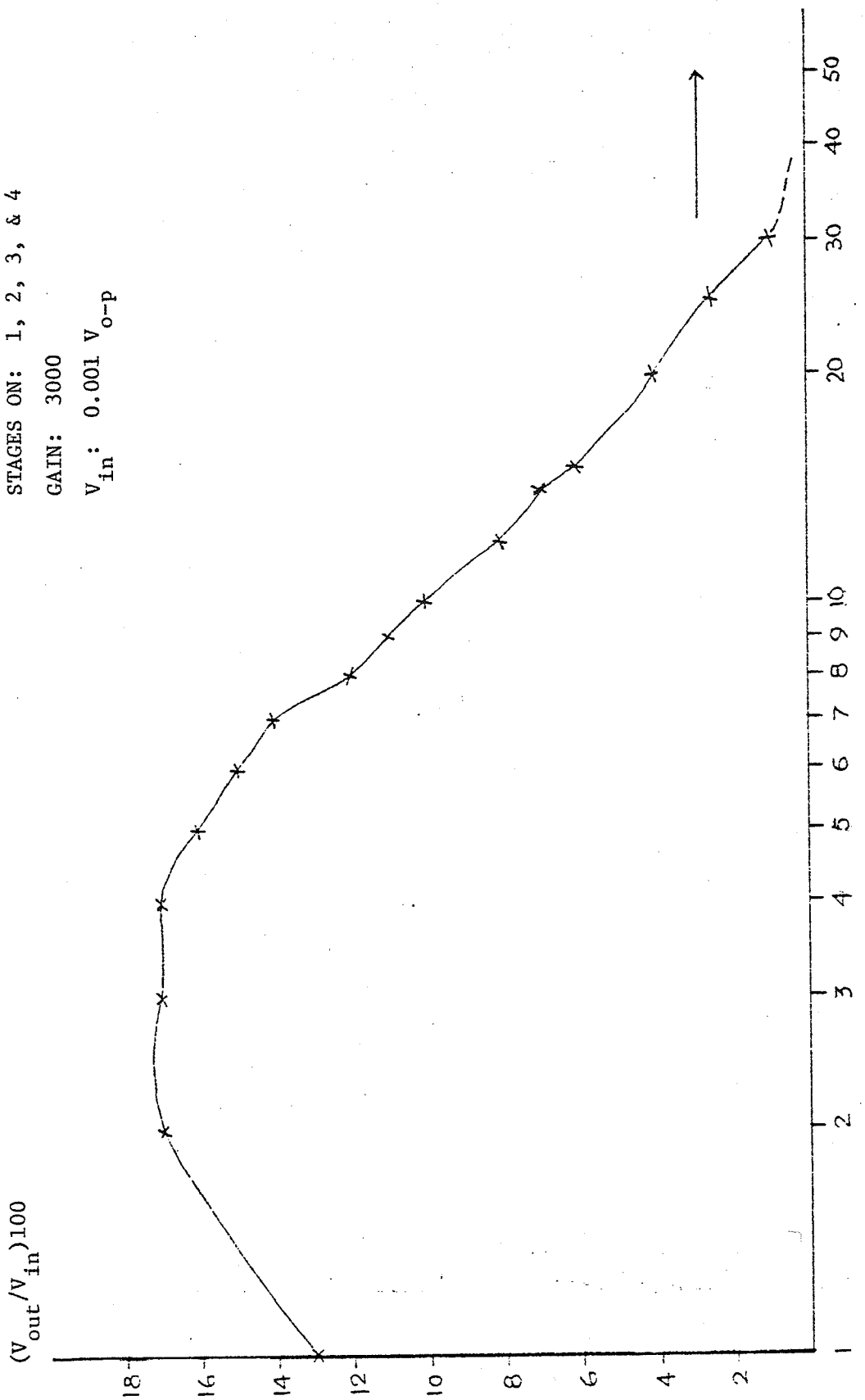


Figure 4-19(a): Frequency Response of Programmable Gain Amplifier

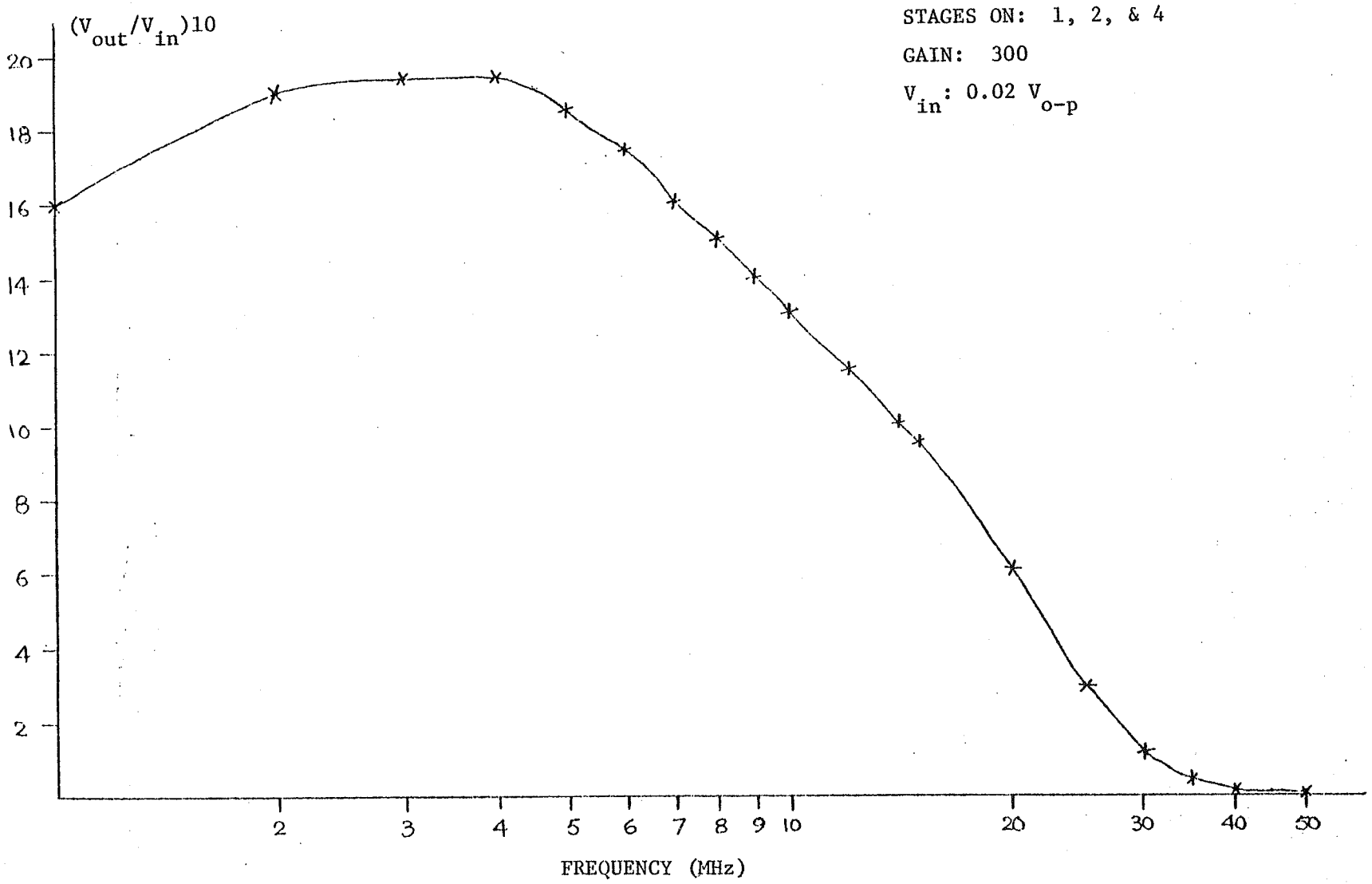


Figure 4-19(b): Frequency Response of Programmable Gain Amplifier

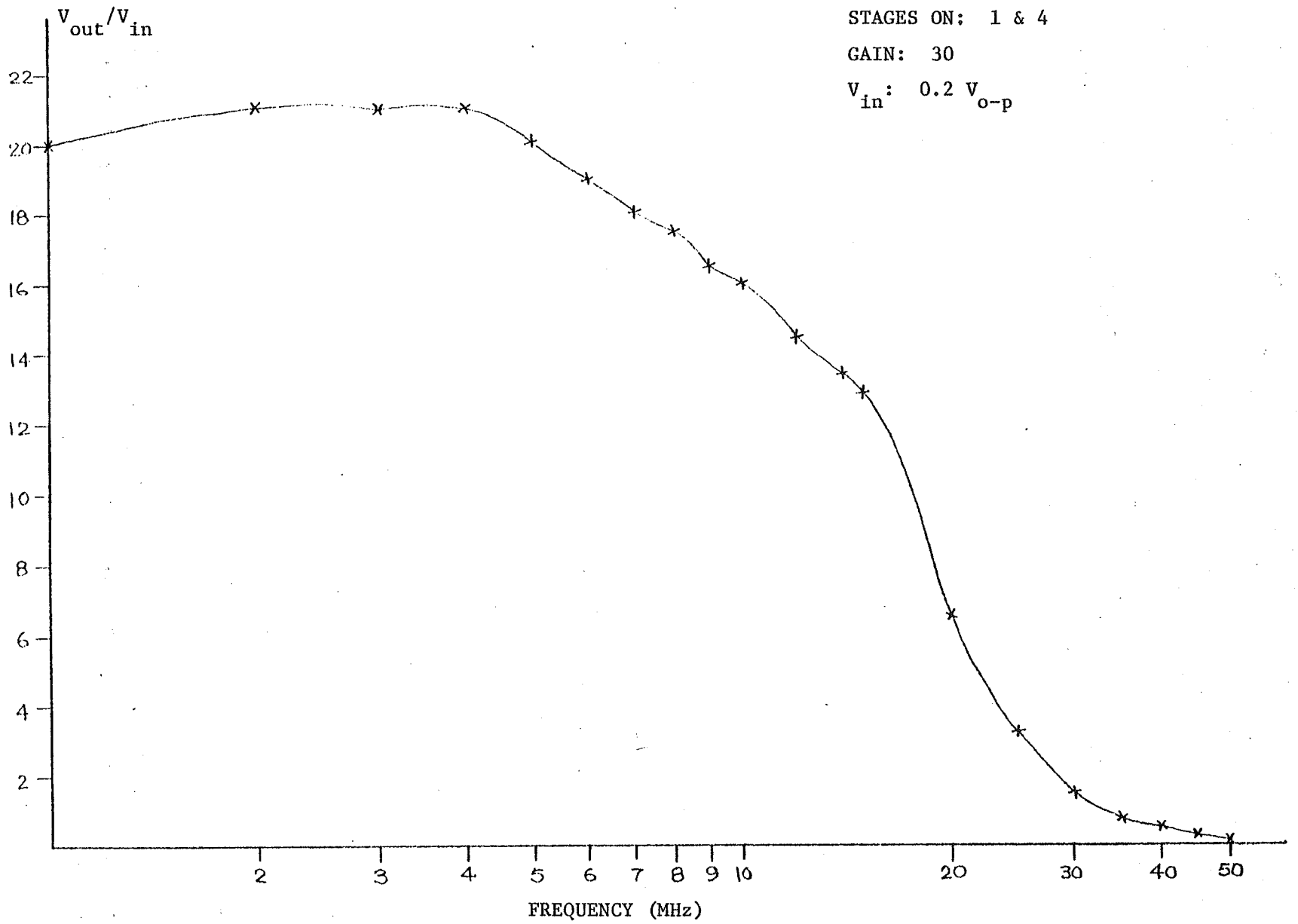


Figure 4-19(c): Frequency Response of Programmable Gain Amplifier

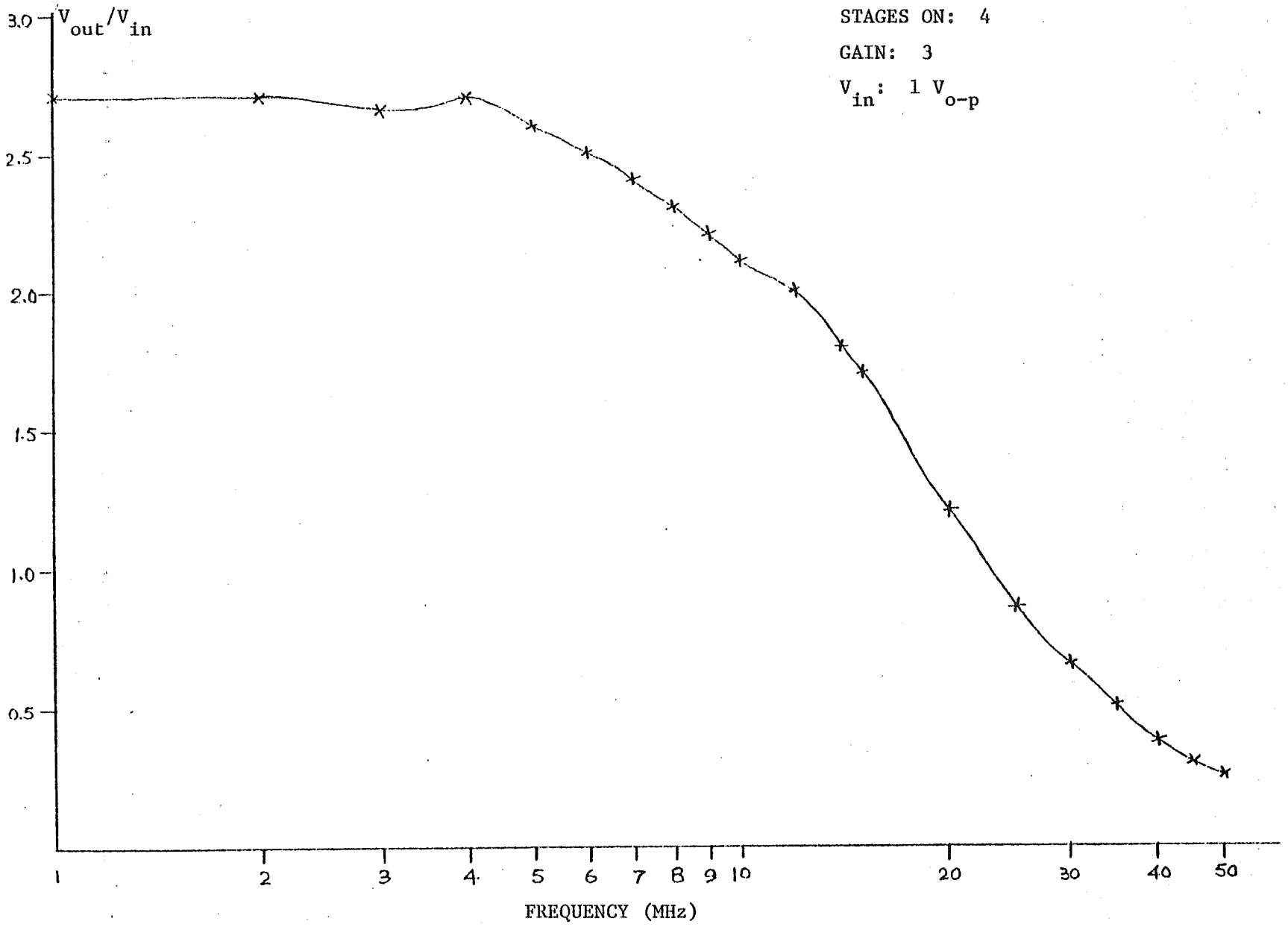


Figure 4-19(d): Frequency Response of Programmable Gain Amplifier

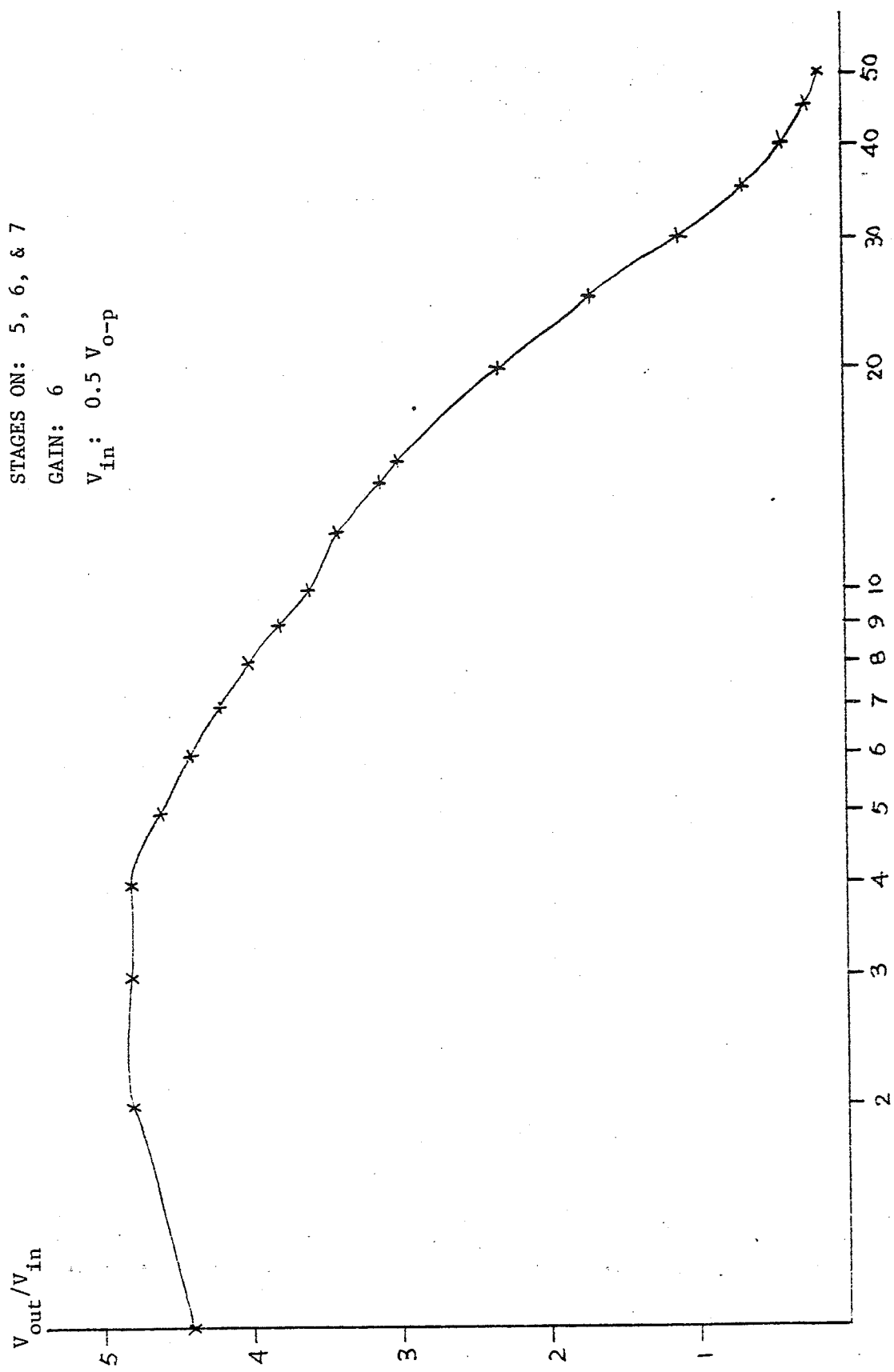


Figure 4-19(e): Frequency Response of Programmable Gain Amplifier

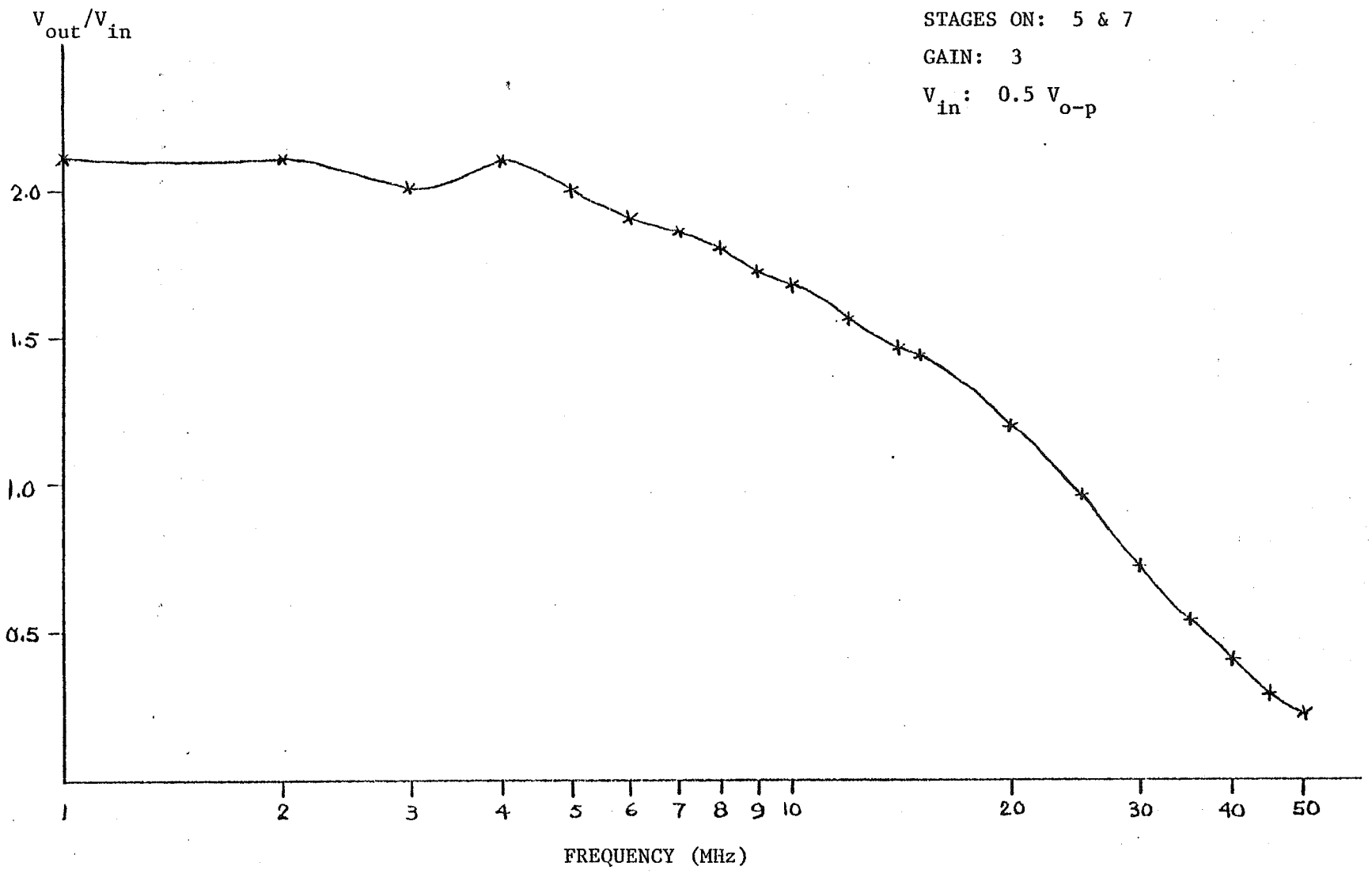


Figure 4-19(f): Frequency Response of Programmable Gain Amplifier

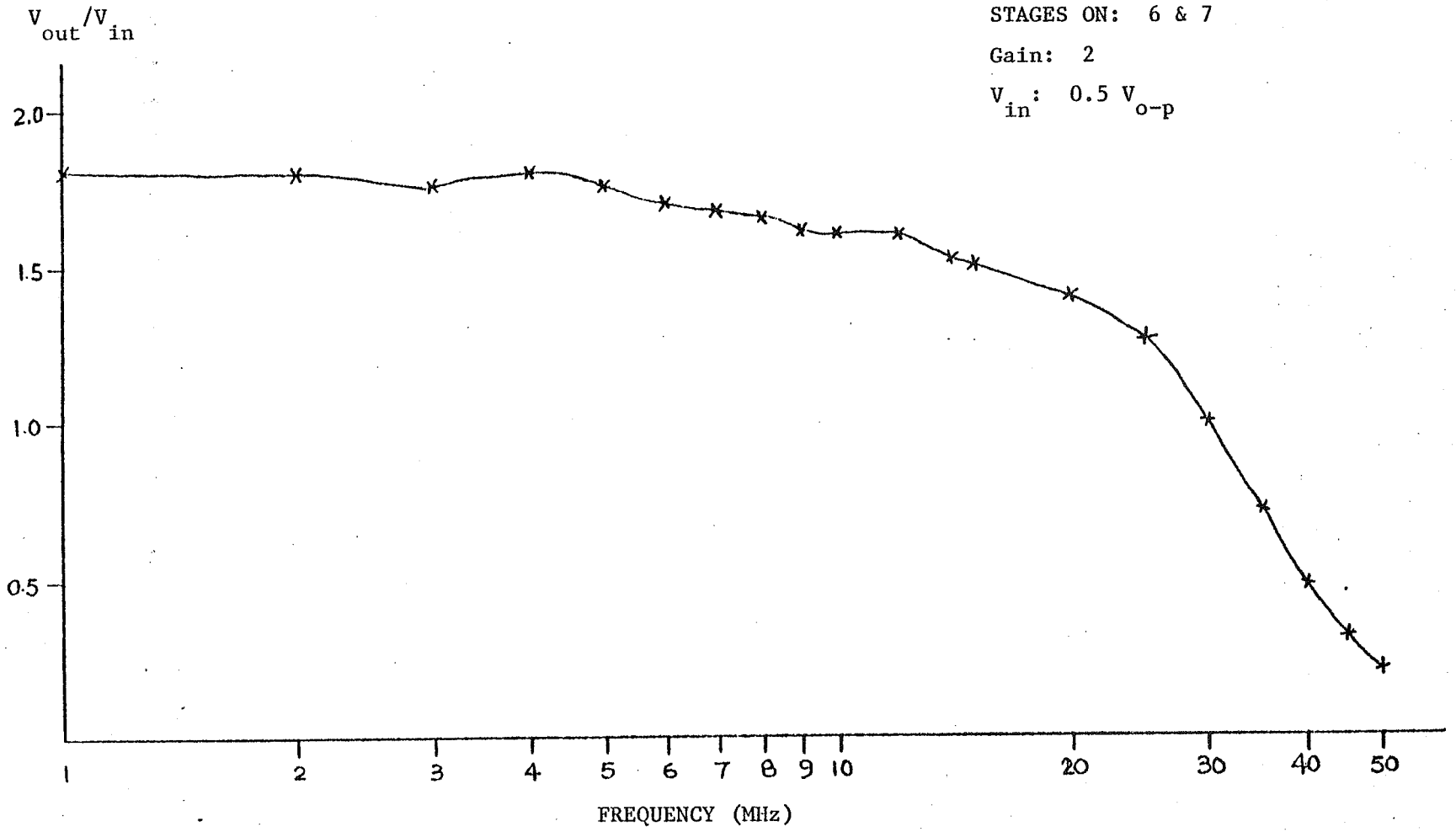


Figure 4-19(g): Frequency Response of Programmable Gain Amplifier

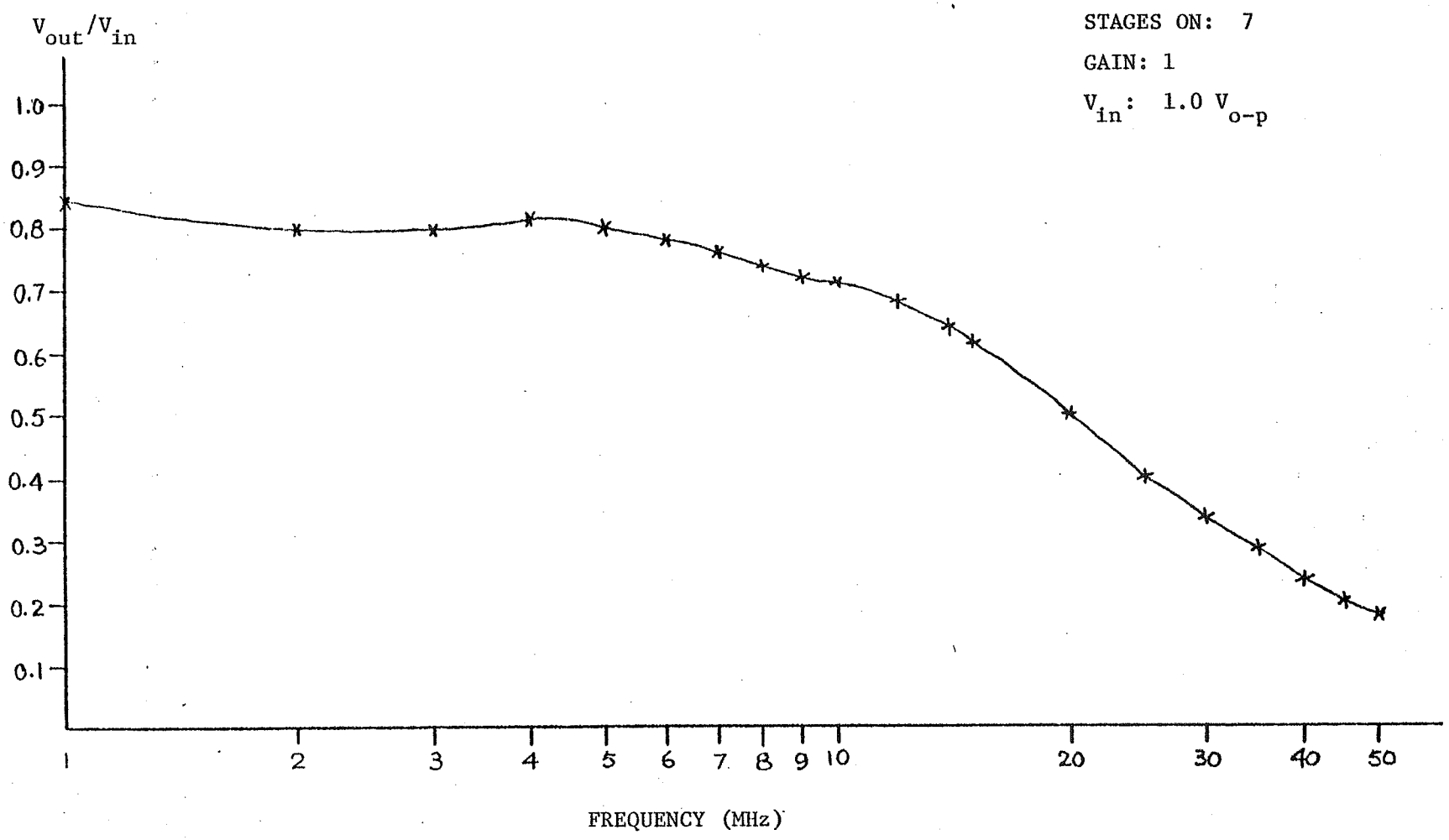


Figure 4-19(h): Frequency Response of Programmable Gain Amplifier

Table 4-4: Noise Level Measurements of Programmable Gain Amplifier with Spectrum Analyser

GAIN	STAGES ON	COMMENTS
3000	1,2,3, & 4	1.6 mV max at 2 MHz
		-10 dB at 20 MHz
		-20 dB at 28 MHz
		-30 dB at 32 MHz
		-40 dB at 37 MHz
		Approximate bandwidth = 38 MHz
300	1,2, & 4	0.16 mV max at 2 MHz
		-10 dB at 23 MHz
		-20 dB at 30 MHz
		Approxmiate bandwidth = 30 MHz
30	1 & 4	16 μV from 2 MHz to 25 MHz
		Approximate bandwidth = 25 MHz
3	4	Noise level not detectable, below noise level of spectrum analyser
6	5,6, & 7	60 μV from 2 MHz to 10 MHz
		-10 dB at 40 MHz
		-20 dB at 50 MHz
		Approximate bandwidth = 30 MHz
3	5 & 7	30 μV from 5 MHz to 15 MHz
		-10 dB at 40 MHz
		Approximate bandwidth = 40 MHz
2	6 & 7	30 μV from 1 MHz to 30 MHz
		-10 dB at 60 MHz
		Approximate bandwidth = 60 MHz
1	7	Noise level not detectable, below noise level of spectrum analyser

* All noise level measurements were made with 300 kHz bandwidth setting on spectrum analyser (Spectrum analyser composes of HP 8553B spectrum analyser RF section, HP 8552A spectrum analyser IF section and HP 1408 oscilloscope)

Table 4-5: Noise Level Measurement of Programmable Gain Amplifier with 250 MHz Scope

GAIN	STAGES ON	NOISE LEVEL (V_{p-p})
3000	1,2,3,& 4	0.4
300	1,2, & 4	0.06
30	1 & 4	0.01
3	4	0.01
6	5,6, & 7	0.002
3	5 & 7	0.001
2	6 & 7	0.001
1	7	not detectable

4.1.13 Pulse Height Detector

4.1.13.1 Device Description

This device essentially detects the absolute pulse height of the received ultrasound signal after being amplified by the HP 461A amplifier and the programmable gain amplifier. The programmable amplifier output signal is half-wave rectified by a diode and the rectified signal charge up a sampling capacitor. The capacitor output voltage drives a FET input voltage follower. A FET input voltage follower is essential in order to reduce leakage. The follower output drives another inverting amplifier stage with a bias adjustment to compensate for the diode voltage drop so that the resultant DC output is as close as possible to the pulse height of the programmable gain amplifier output signal. Input to the pulse height detector is AC coupled to block off any possible offset from the programmable gain amplifier output. The sampling capacitor is discharged by a CMOS analog switch at the falling edge of the channel A output of the clipper. If this automatic discharge feature is disabled by the computer, the computer can discharge the sampling capacitor by writing into bit 0 of the pulse height detector control status register PHD-CSR.

4.1.13.2 Circuit Description

The pulse height detector circuit is located on Board A13 (Figure A-12 of Appendix A). At the input section of the pulse height detector circuit, the 0.1 μF capactor and the 49.9 Ω resistor provide AC coupling to the output signal of the programmable gain amplifier. The 49.9 Ω resistor also provides a termination of about 50 Ω to the input signal. The input signal is rectified by the diode and charges up the 200 pF smapling capacitor. The 825 Ω resistor limits the current through the diode to about 10 mA at 10 V input. The 825 Ω resistor

and the 200 pF capacitor are designed to charge up the 200 pF capacitor in 99 cycles with a 30 MHz signal. The fact that the design was based on a 30 MHz signal is because the programmable attenuator has a 30 MHz maximum rating. The 200 pF sampling capacitor drives a FET input voltage follower (μA 740 operational amplifier). The output inverting amplifier is implemented by the LM 318 operational amplifier and the diode drop compensation bias is accomplished by the 4.7 V zener diode with bias adjustment controlled by the 10 kΩ trim pot. The sampling capacitor is discharged by closing a CMOS analog switch (DG 381CJ). The 511 Ω resistor to the switch is for limiting current through the switch. The switch is closed by a 1 μs TTL pulse (PHD RESET).

4.1.13.3 Controller

4.1.13.3.1 Control Word Format and Programming Guide

Figure 4-20 gives the control word format of the pulse height detector. A "1" in bit 0 of the PHD-CSR will generate a 1 μs pulse to discharge the sampling capacitor of the pulse height detector. The automatic reset feature is enabled by writing a "1" into bit 1. During automatic reset mode, the 1 μs reset pulse is triggered by the falling edge of the clipper's channel A output. The pulse height detector controller also has the capability of detecting the falling edge at the channel B output of the clipper circuit and generate a positive trigger pulse of 1 μs to the A/D clock input of the 7/32 computer. For the analog input channel to respond to the trigger pulse, bit 2 must be set to "0."

4.1.13.3.2 Controller Circuit Description

The controller is located on Board D8 (Figure A-13 of Appendix A). $\overline{\text{DEV 6}}$ is the signal as a result of decoding the four most significant bits of the DIO

PHD-CSR (Write only)
Addr = 000

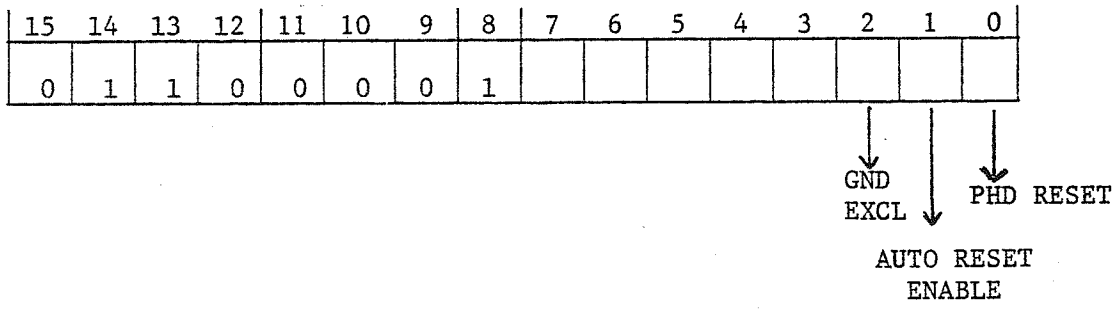


Figure 4-20: Control Word Format for the Pulse Height Detector

output. Thus during write mode, a strobe pulse (derived from DOPDA) is routed to pin 15 of the demultiplexor IC(AY). This strobe pulse is routed to pin 4 of IC(CV) if bit 0 of PHD-DSR is set and to pin 3 of IC(DX) and pin 3 of IC(BZ) as a clock pulse to latch bits 1 and 2 of PHD-CSR. Setting bit 1 of PHD-CSR to logic 1 will gate the 1 μs automatic reset pulse to pin 6 of IC(CV). The 1 μs automatic reset pulse is triggered by the falling edge of the channel A output (STATE A) of the clipper circuit. Setting bit 2 of PHD-CSR to logic 0 will enable the A/D input channel to respond to the trigger clock pulse EX CLOCK which is triggered by the falling edge of the channel B output (STATE B) of the clipper circuit. The inverted EX CLOCK signal at pin 4 of IC(DY) is reinverted by the 50 Ω line-driver IC(DW) as SIGNAL RECIEVED. This signal allows the user to trigger the TRW 9-BIT video A/D channel.

4.1.13.4 Performance Evaluations

Since the programmable attenuator has a maximum rating of 30 MHz, the pulse height detector was designed basing on a 30 MHz maximum frequency and the sampling

capacitor should be charged up to follow the signal peak in 99 cycles with a 30 MHz signal. The pulse height detector was tested by amplifying the tone burst signal at the output of the mixer with the programmable gain amplifier. The amplifier drives the pulse height detector input and the amplifier gain was adjusted to give a maximum signal. Table 4-6 gives the observaed number of cycles required to charge up the sampling capacitor at different frequencies up to 30 MHz. It was also observed that the pulse height detector can follow signal peaks from 1.2 V to 12 V, i.e., a dynamic range of 20 dB. Since there is an inverting amplifier at the output section of the pulse height detector, the output DC voltage is negative polarity.

Table 4-6: Pulse Height Detector Performance

FREQUENCY (MHz)	NO. OF CYCLES
1,2,3	8
4	16
5,6,7,8,9,10,11,12	32
13,14,15,20,30	64

4.1.14 Carrier Frequency, Pulse Repitition Frequency, and Pulse Width (Cycles) Display

4.1.14.1 Device Description

This board contains the 7-segment LED displays BCD to 7-segment decoders (SN 74LS47) and LED current limiting resistor blocks. This board displays the carrier frequency of the tone-burst signal generated (ten digits), the pulse

repitition frequency of the tone-burst signal (four digits) and the pulse width (no. of cycles) of the tone-burst signal (four digits).

4.1.14.2 Circuit Description

This display board is mounted at the back of the system front panel. The displays are generated as a result of the SN 74LS47 BCD to 7-segment decoders decoding the BCD inputs from the window status display generator board (Board A0) and the carrier frequency display latch (Board D4). For each of the display, the BCD to 7-segment decoders are connected in order to provide leading zero blanking effects. See Figure A-15 of Appendix A.

4.2 The Power System

4.2.1 The Main System Supply

The power supply module provides all the voltages required for the operation of the data acquisition system. The module supplies the three voltages used by the circuits, i.e., the digital supply and two analog supplies. One additional power supply in the module provides the power used in the system front panel displays. The power supply module is self contained and has two controls. The module is energized by the switch on the front panel of the module and the brightness of the system front panel display can be varied by a knob on the back of the power supply module.

The digital supply is implemented with a Power-one model E 15-9 regulated power supply. This supply is fused on the AC line and contains both overload protection and short circuit protection. The digital supply is set to deliver 12 volts to the circuits up to 10.2 amperes. The analog supplies delivers both a positive and a negative 24 volts up to 7.2 amperes to the circuit. This section

is implemented with two Power-one model E 24-7.2 regulated power supplies. The two supplies are fused on the AC line and both provide overload and shortcircuit protection. See Figure A-16 of Appendix A for the supply connections.

The power supply that powers the system front panel displays has an adjustment knob on the back panel of the power supply module to allow the user to vary the voltage of this display supply between 2 volts and 5 volts. A schematic for this display power supply is given in Figure A-17 of Appendix A. The circuit of this regulated supply consists of a precision voltage reference and a series pass regulator. The regulator section includes over-current and reverse voltage protection.

The voltage reference for the display supply is implemented with the zener diode. An LM 741 operational amplifier senses the voltage produced by the zener diode and controls the zener voltage by limiting the current available to the zener diode. This reference voltage is attenuated by the back panel adjust knob and used to set the regulated output voltage.

The pass regulator section of the display supply consists of an LM 741 operational amplifier and a darlington transistor pass element. The operational amplifier provides voltage gain and feedback regulation and the darlington pair provides current gain. The output current is monitored and when it exceeds 5 amperes, the 2N2483 transistor turns on and reduces the drive from the darlington pass element.

4.2.2 On-board Power Supply System

Voltage regulators are used on every circuit board of the data acquisition system. These voltage regulators are driven by the three supply voltages (+12 V, +24 V, and -24 V) of the power supply module. As all the circuit boards are

mounted on a card rack with a back plane, these voltage regulators provides good local regulation on every circuit board and eliminates noise problem due to the long power bus on the back plane.

Chapter 5

System Evaluation

The data acquisition system was tested by performing time-of-flight and attenuation measurements. The test was performed by using a tank with two comparments with an acoustical window in between. One tank was filled with water and the other with manganese sulphate solution. To each of the tanks was mounted a 0.5 MHz fundamental barium titanite transducer and the distance between the transducers was fixed. A motor and gear train was used to move the two transducers with a constant velocity.

For measuring attenuation, the transducers were moved at a velocity of 0.07620 cm s^{-1}. A tone burst signal of 2.5 MHz carrier frequency was generated to drive the transmit transducer. The received signal was amplified by the HP 461A amplifier, through the 20 MHz low pass filter, and amplified again by the programmable gain amplifier to drive the pulse height detector. The pulse height detector output was digitized by the A/D converter of the 7/32 computer. The natural log of the digitized pulse height detector output was plotted against distance and Figure 5-1(a) and (b) give the plots in two measurements. From Figure 5-1(a) and (b), a linear relationship between the natural log of the received pulse height and distance was observed. This linear relationship was expected and the attenuation of manganese sulphate obtained from the slope of the straight line of Figure 5-1(a) and (b) are 0.0376 Np cm^{-1} and 0.0428 Np cm^{-1} respectively.

Time-of-flight measurement was performed by moving the transducers at a velocity of 7.62×10^{-3} cm s^{-1} and the tone burst carrier frequency used was 1.5 MHz. The HP 5328A universal counter was set to the time interval averaging mode

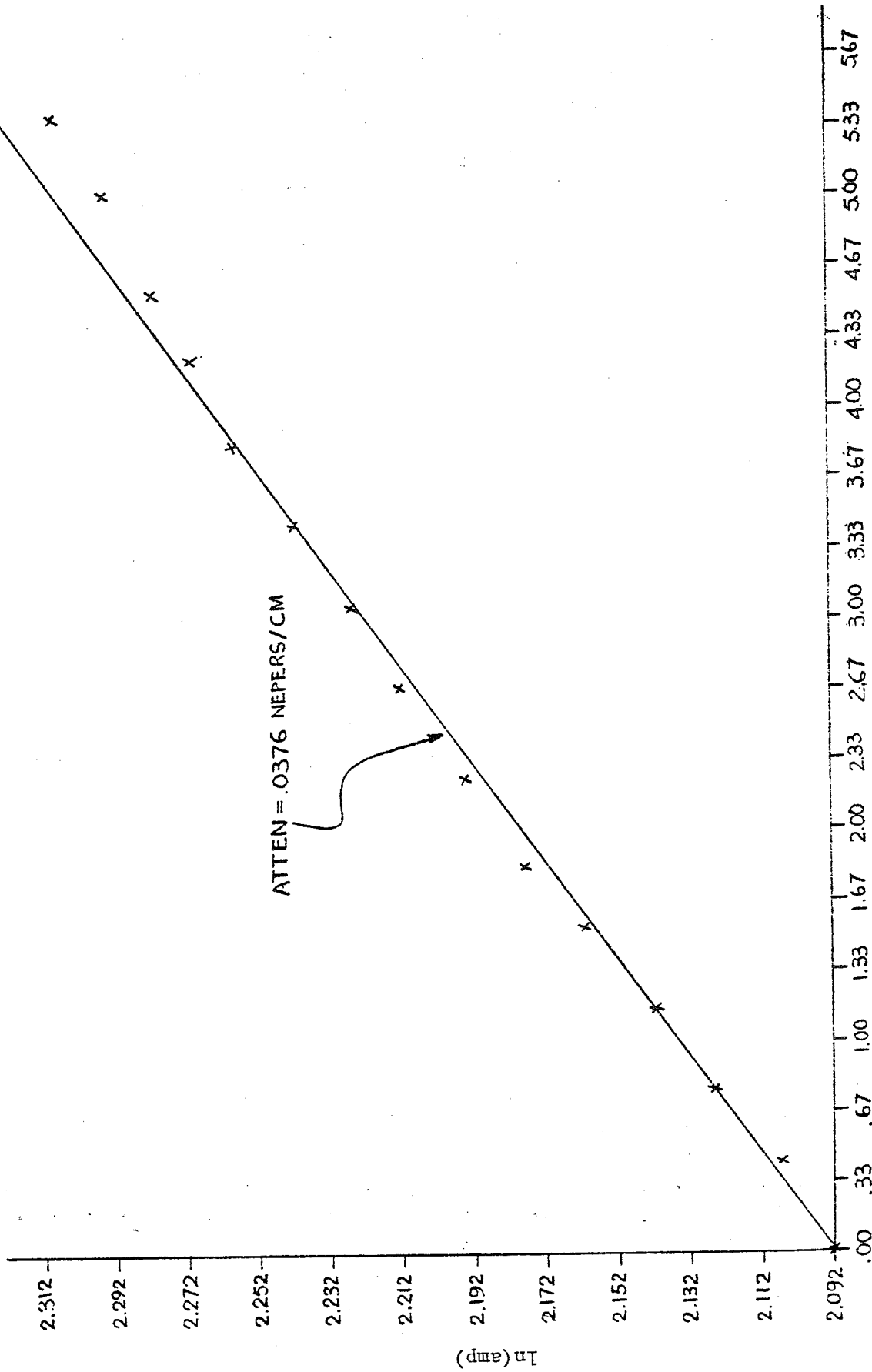


Figure 5-1(a): Attenuation Measurement of Manganese Sulphate

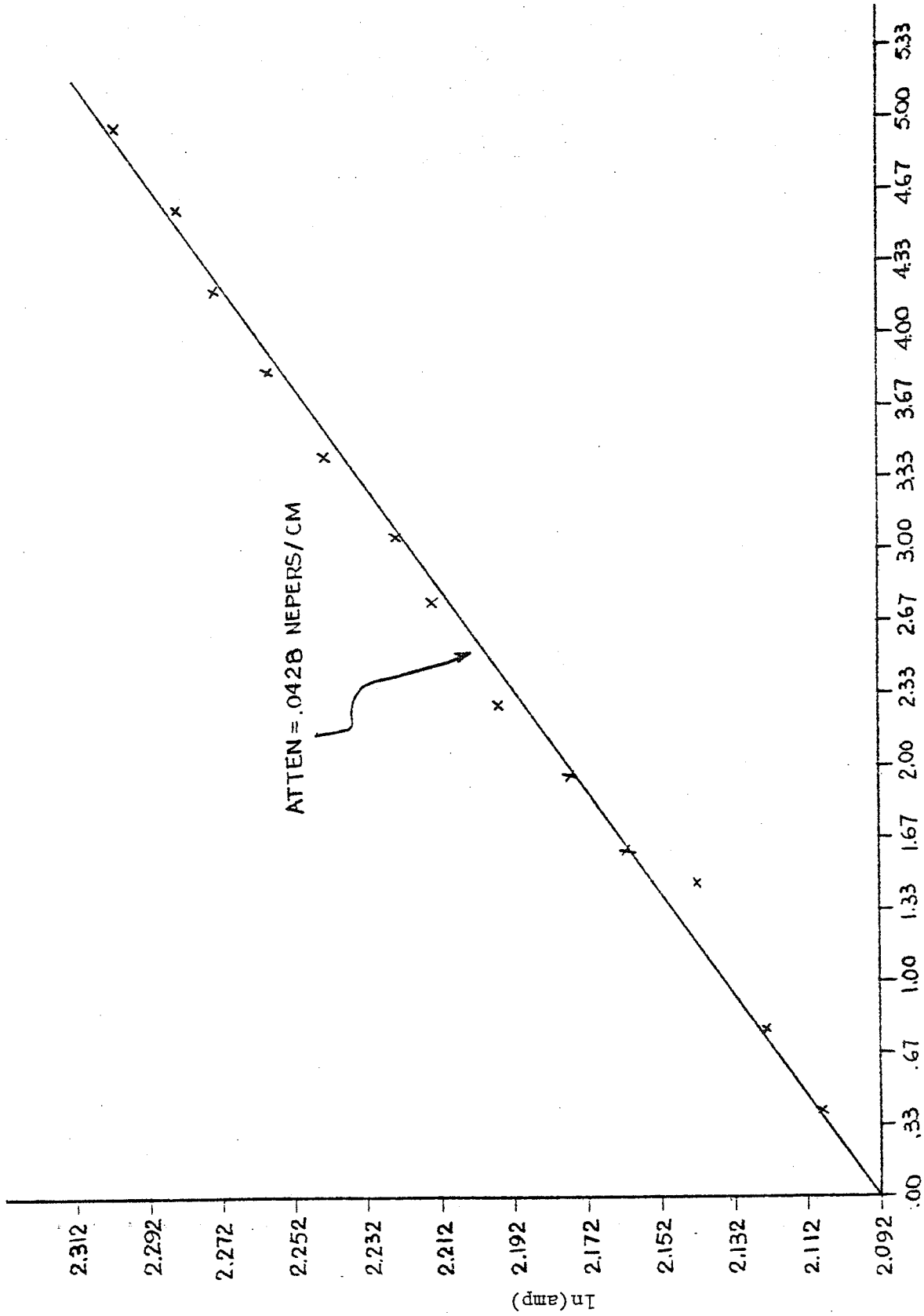


Figure 5-1(b): Attenuation Measurement of Manganese Sulphate

mode of averaging 100 samples. As the tranducers moved, time-of-flight was recorded from the counter every five seconds. Time-of-flight was plotted against distance and a linear relationship between time-of-flight and distance was observed in two measurements. Figures 5-2(a) and (b) shows the time-of-flight against distance plots and from the slope of these straight lines, the velocity of sound through the manganese sulphate solution was found to be 1508 $m\ s^{-1}$ in both cases.

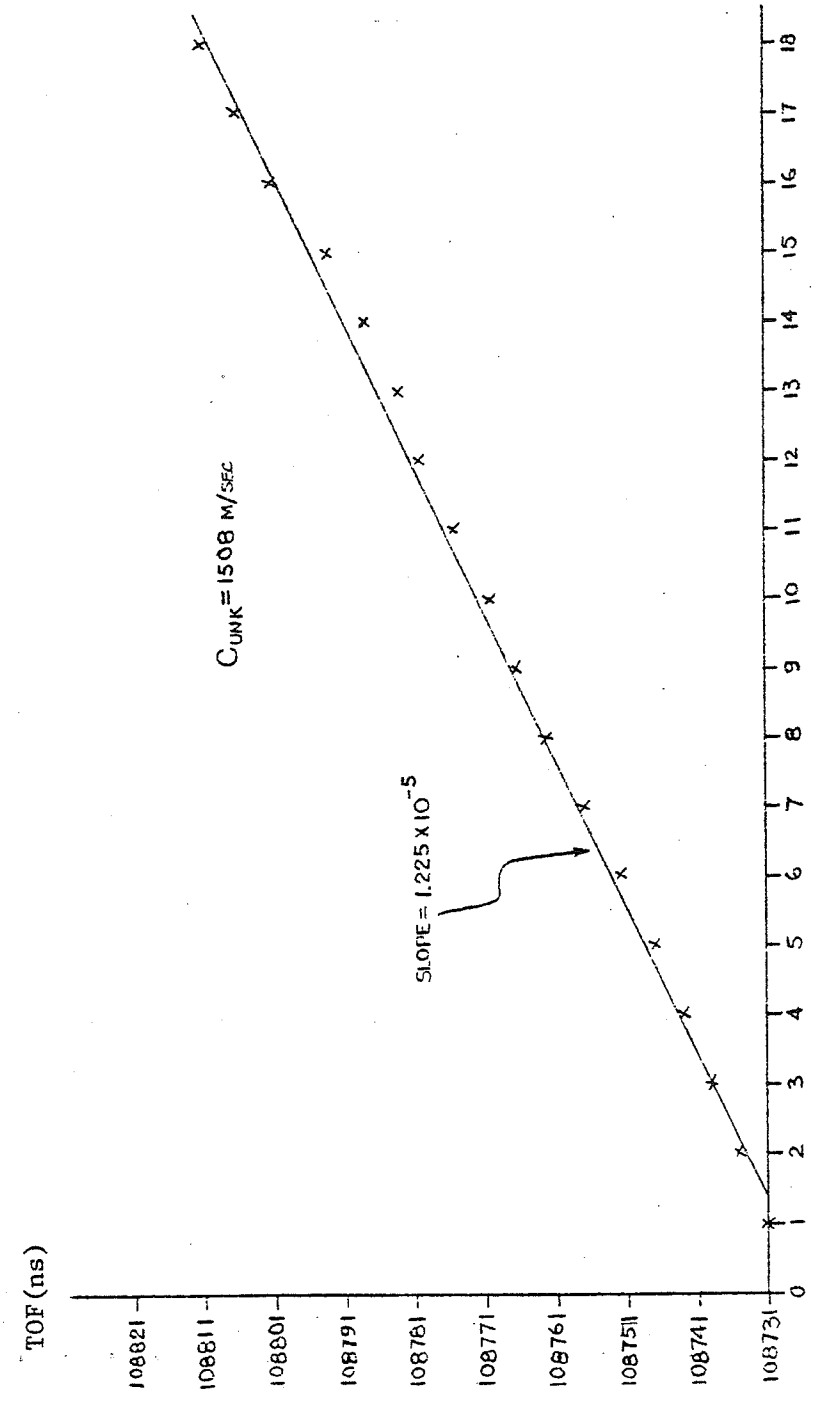


Figure 5-2(a): Velocity Measurement of Manganese Sulphate

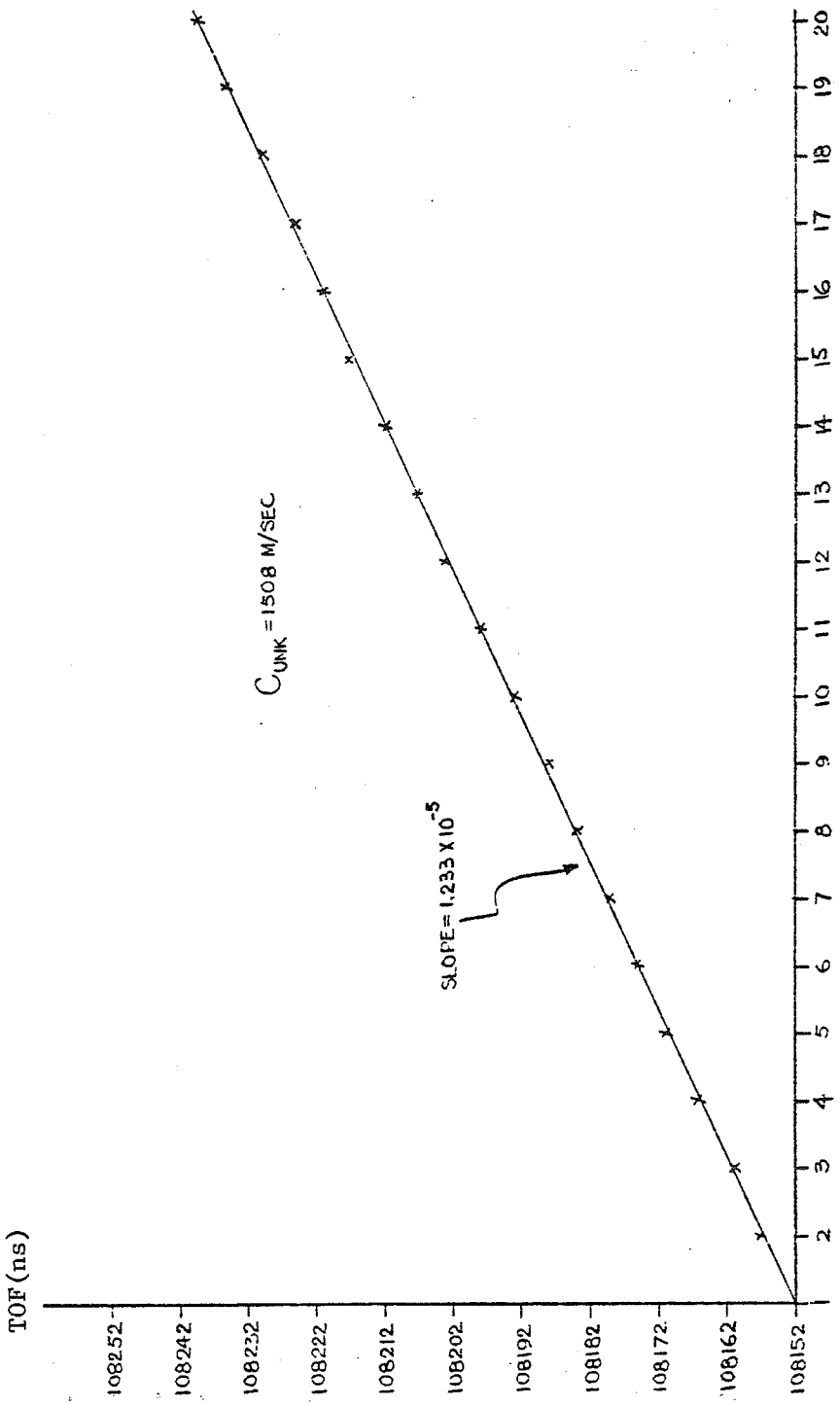


Figure 5-2(b): Velocity Measurement of Manganese Sulphate

Chapter 6

Recommendations for System Improvement

The following are suggestions which might up grade the present data acquisition system:

6.1 Programmable Window Generator

This device is implemented with TTL logic circuits. Except the repetition frequency generator, the synchronizer and the cycle selector are implemented by schottky TTL logic to minimize gate delay. The analog element, i.e., the zero crossing detector uses an ECL voltage comparator. The programmable window generator can actually be implemented entirely with ECL logic circuits. If the whole circuit is built on a printed circuit board with a good ground plane and short connections, the maximum operational frequency with different cycle selections might be improved. In addition, ECL has faster rise-time and fall-time. This might eliminate the sharp edges at the end of the coherent tone-burst (see performance evaluation of window generator in section 4.1.2.4 of Chapter 4) as a result of the constant 10 ns fall-time of the window. Instead of cable delay lines, variable digital delays might be used to accurately "trim" the window zero-crossing to coincide with the zero-crossing of the synthesizer signal.

6.2 Programmable Attenuator

This device is already fabricated on a printed circuit board with a good ground plane. However, some of the connection leads are a little too long. Should this circuit be lay-out again with shorter connection leads, a better

frequency response might be possible.

6.3 Clipper

The clipper works well up to 50 MHz with 5 ns rise-time and 3.5 ns fall-time. However, it might be a good idea to fabricate the whole circuit on a printed circuit board with a good ground plane. This might give a square wave with less undershoot at the voltage comparator output at the high frequencies.

6.4 Programmable Gain Amplifier

Teledyne Philbrick's 1435 operational amplifier (1 GHz gain bandwidth) and Datel's AM 500 operation amplifier (100 MHz gain bandwidth) are used in the implementation of the programmable gain amplifier. The 1435 doesn't have a very good slew rate and output swing and (slew rate = 300 V/μs, output range = $\pm$ 7 V) the output current drive is only $\pm$ 14 mA. A better frequency response might be possible if the 1435 be replaced by a better performance device. Burr Brown's 3554 (not available during development stage of the data acquisition system) might be a solution as it has 1.7 GHz gain bandwidth, 1000 V/μs slew rate and an output voltage range of $\pm$ 11 V at $\pm$ 125 mA. Its higher current drive and high input impedance ($10^{11}\Omega$) also reduces resistance values in the amplifier circuit and improves the frequency response due to stray capacitance.

In the present implementation with the 1435 and AM 500 operational amplifiers, printed circuit boards are used. However, some of the connections might still be a little long and shorter connections might improve the present frequency response.

6.5 Interface with Perkin Elmer 7/32 Computer

In the present configuration, the digital input/output (DIO) serve as the only communication hardward between the 7/32 and the data acquisition system. Due to this limited hardware resource, an external processor bus (the system controller) is implemented for communications between the different system devices in the data acquisition system and the DIO. This configuration particularly slows down the reading process as the user has to write into the 16 bit output specifying a read mode before outputs of the addressed system device can be read through the 16 bit input. A speed-up might be possible by using more DIO's or to interface the system devices directly into the 7/32's system bus and using memory mapped I/O.

List of References

1. Foster. S. G. (1980). Thesis for the degree of Master of Science in Electrical Engineering, University of Illinois.
2. Hewlett Packard (1974). "Programming in Detail," Programming the 8660A/B Synthesized Signal Generator (Standard BCD Interface), Hewlett Packard Application Note 164-1, Chapter 3, p. 5-7.
3. Hewlett Packard (1974). "Interface Specifications," Programming the 8660A/B Synthesized Signal Generator (Standard BCD Interface), Hewlett Packard Application Note 164-1, Chapter 4, p. 10.
4. Hewlett Parkard (1974). "Interface Specifications," Programming the 8660A/B Synthesized Signal Generator (Standard BCD Interface), Hewlett Packard Application Note 164-1, Chapter 4, p. 12.
5. Hewlett Packard (1976). Manual for the Special Option H03 of the 5328A Counter.
6. Hewlett Packard (1971). Models 10514 A/B/C and Models 10534 A/B/C 0.05 - 500 MHz Double Balanced Mixers, Hewlett Packard Technical Data.
7. Hewlett Packard (1963). Operating and Service Manual of the Wide Band Amplifier 461A.

Appendix A

Schematics

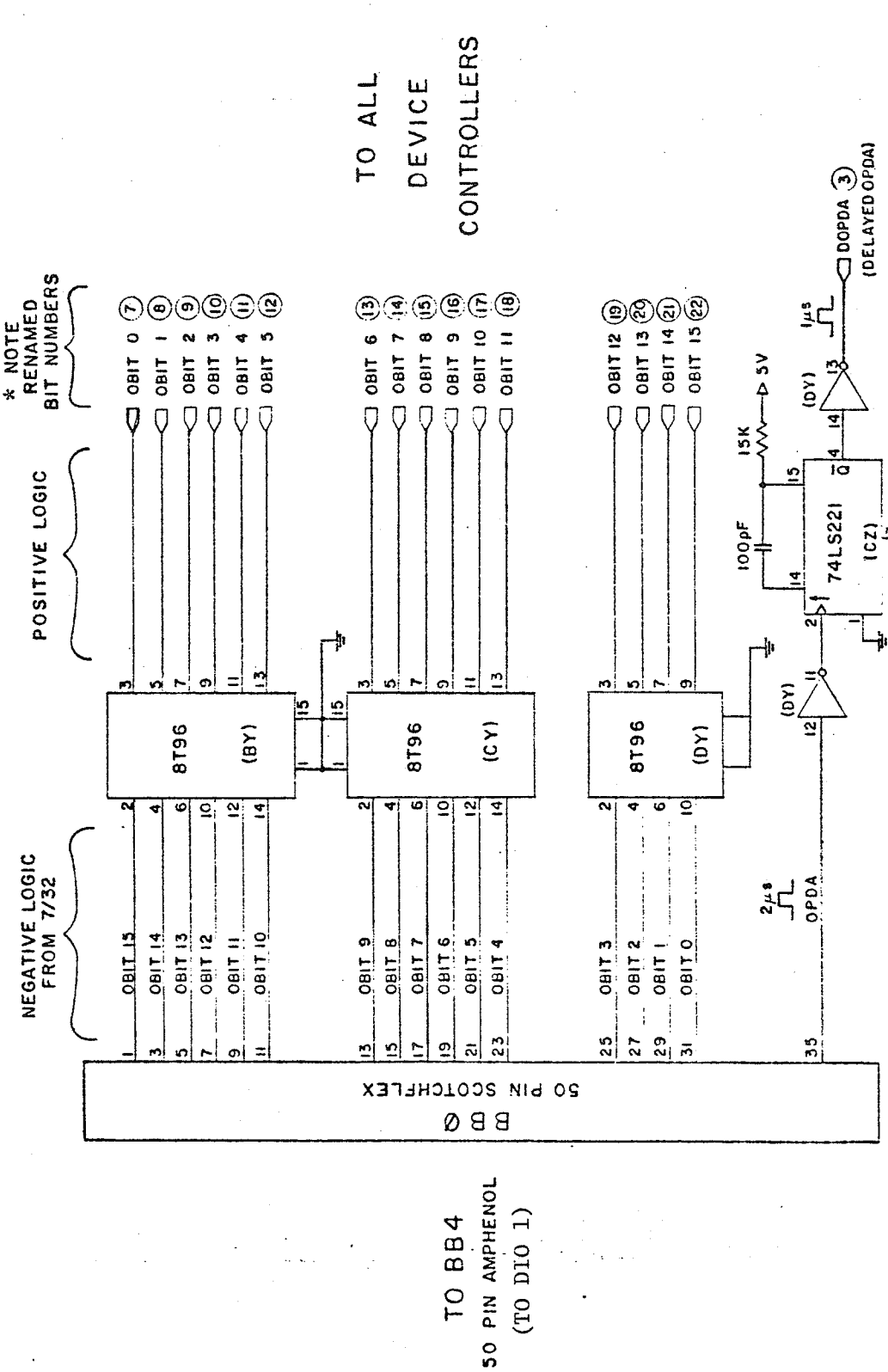


Figure A-1(a): Positive Logic Converter and OPDA Delay Logic (Board D2)

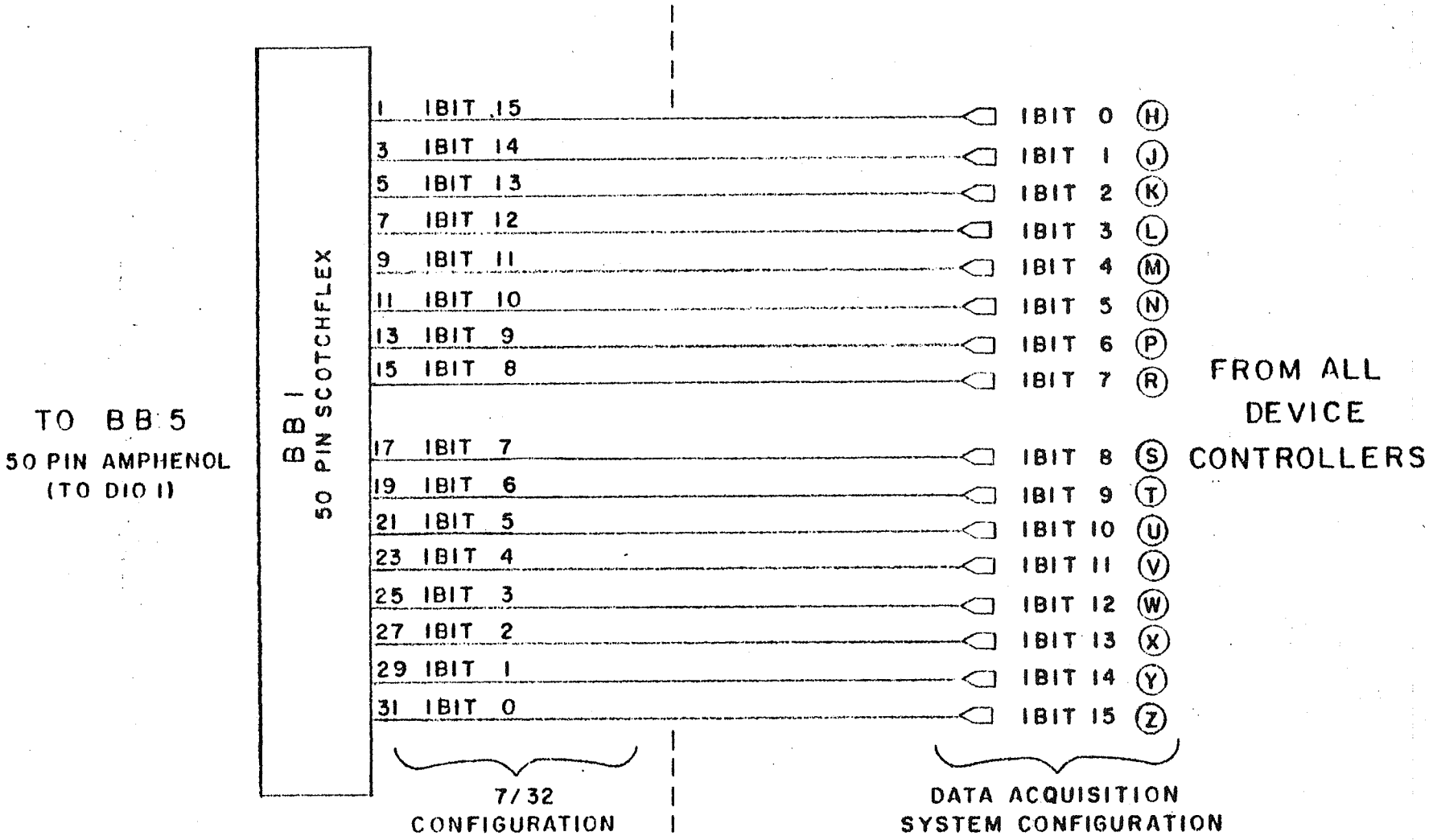


Figure A-1(b): DIO 1 16 Bit Input Interface (Board D2)

SIGNAL (7/32 CONFIGURATION)	BB5,LL2 (50 PIN AMP)	BB1, BB3 (50 PIN SCOTCHFLEX)
IBIT 15	1	1
GND	18	2
IBIT 14	2	3
GND	19	4
IBIT 13	3	5
GND	20	6
IBIT 12	4	7
GND	21	8
IBIT 11	5	9
GND	22	10
IBIT 10	6	11
GND	23	12
IBIT 9	7	13
GND	24	14
IBIT 8	8	15
GND	25	16
IBIT 7	9	17
GND	26	18
IBIT 6	10	19
GND	27	20
IBIT 5	11	21
GND	28	22
IBIT 4	12	23
GND	29	24
IBIT 3	13	25
GND	30	26
IBIT 2	14	27
GND	31	28
IBIT 1	15	29
GND	32	30
IBIT 0	11	31
GND	33	32

SIGNAL (7/32 CONFIGURATION)	BB5,LL2 (50 PIN AMP)	BB1,BB3 (50 PIN SCHOTCHFLEX)
IPDR	34,(47)	33
GND	35,(48)	34
IDA	36,(49)	35
GND	37,(50)	36
IPLV	38	37
+5 V	39	39
IBSY	40	41
IHPV	41	43

( ): only for connector LL2

** BB1 to BB5
BB3 to LL2

Figure A-1(c): Corresponding Pin-outs for Connectors BB1 to BB5 and BB3 to LL2.

SIGNAL (7/32 CONFIGURATION)	BB4 and LL1 (50 PIN AMP)	BB0,BB2 (50 PIN SCOTCHFLEX)
OBIT 15	1	1
GND	18	2
OBIT 14	2	3
GND	19	4
OBIT 13	3	5
GND	20	6
OBIT 12	4	7
GND	21	8
OBIT 11	5	9
GND	22	10
OBIT 10	6	11
GND	23	12
OBIT 9	7	13
GND	24	14
OBIT 8	8	15
GND	25	16
OBIT 7	9	17
GND	26	18
OBIT 6	10	19
GND	27	20
OBIT 5	11	21
GND	28	22
OBIT 4	12	23
GND	29	24
OBIT 3	13	25
GND	30	26
OBIT 2	14	27
GND	31	28
OBIT 1	15	29
GND	32	30
OBIT 0	16	31
GND	33	32

SIGNAL (7/32 CONFIGURATION)	BB4 and LL1 (50 PIN AMP)	BB0,BB2 (50 PIN SCOTCHFLEX)
OPDR	34,(47)	33
GND	35,(48)	34
OPDA	36,(49)	35
GND	37,(50)	36
OPLV	38	37
+5 V	39	39
OBSY	40	41
OHPV	41	43

( ): only for connector LL1

** BB0 to BB4
BB2 to LL1

Figure A-1(d): Corresponding Pin-outs of Connector BB0 to BB4 and BB2 to LL1

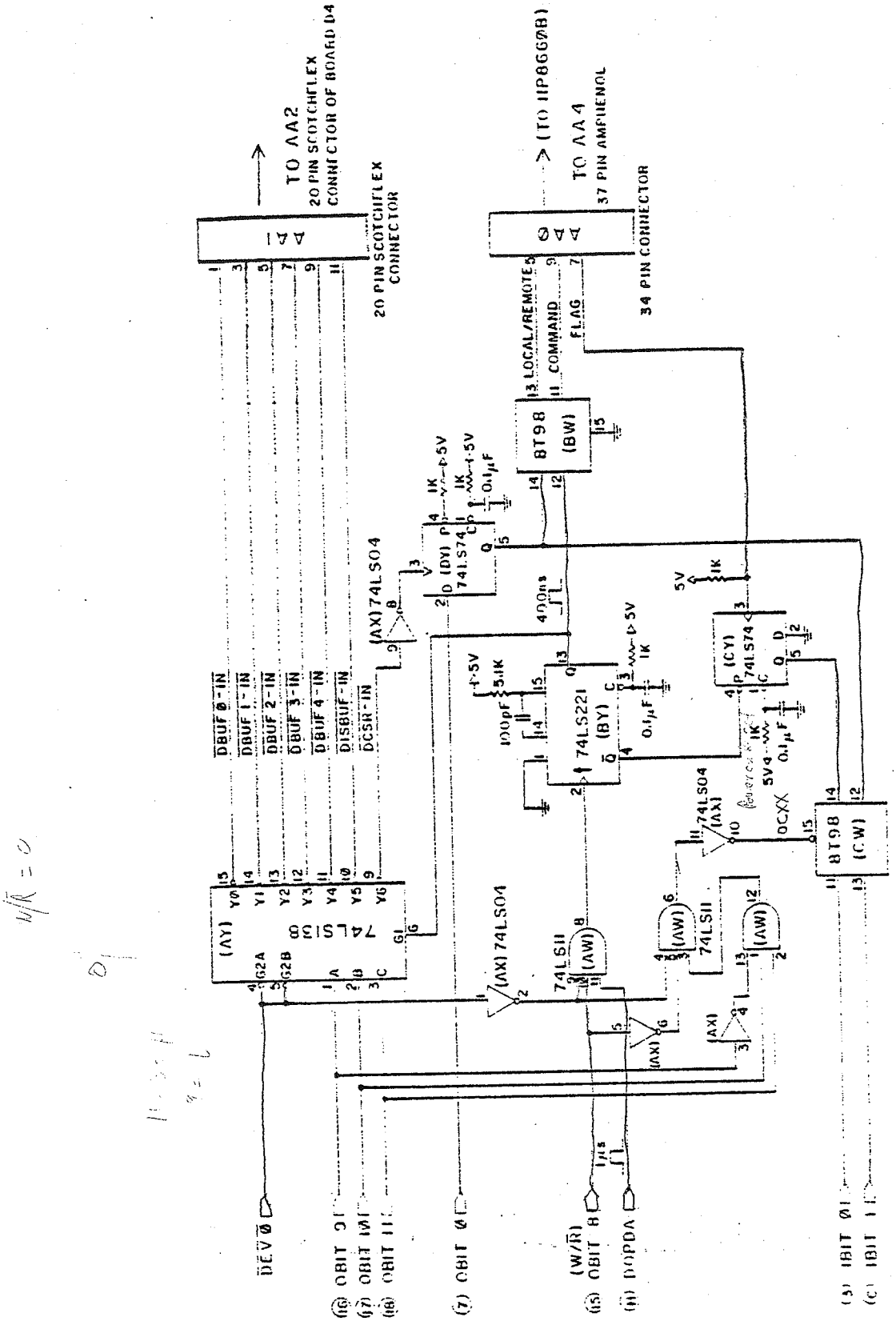


Figure A-2(a): HP 8660B Controller Control Logic (Device 0) (Board D3)

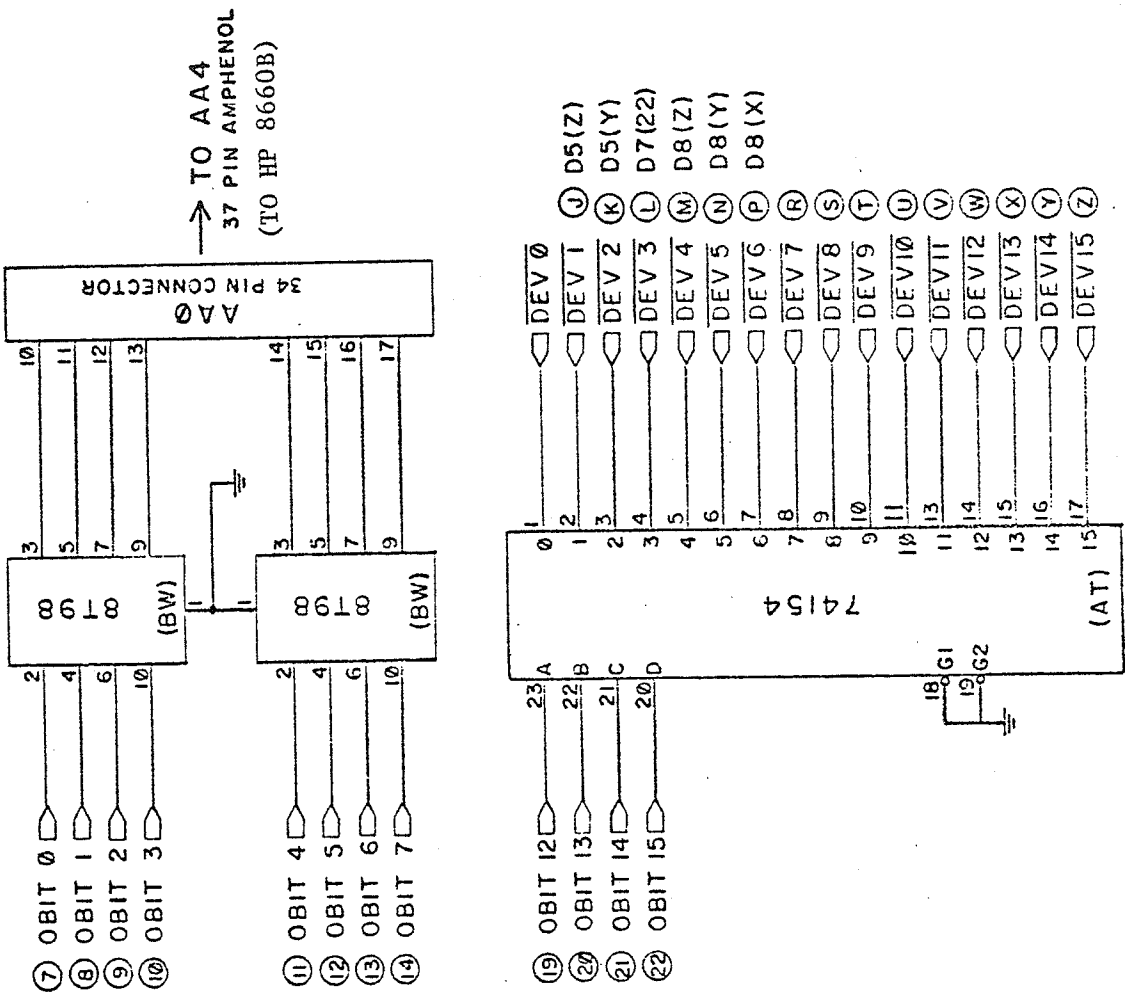


Figure A-2(b): HP 8660B Controller Digit Driver and Device Address Decoder (Board D3)

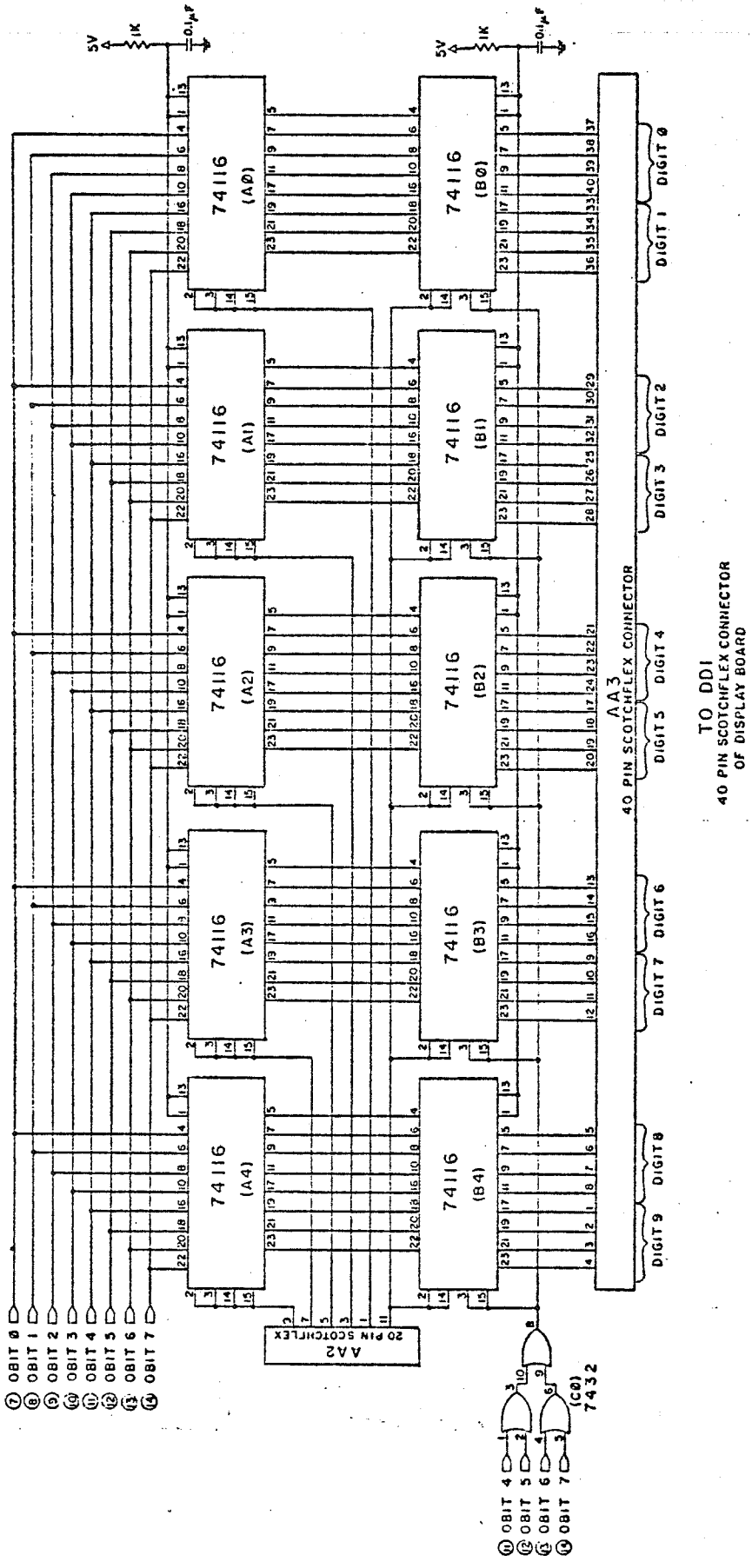


Figure A-2(c): HP 8660B Controller Carrier Frequency Display Latch (Board D4)

FUNCTION	36 PIN BLUE RIBBON J3	37 PIN AMPHENOL AA4	34 PIN SCOTCHFLEX AA0
DIGIT 2-8	28	17	17
DIGIT 2-4	29	16	16
DIGIT 2-2	30	15	15
DIGIT 2-1	31	14	14
DIGIT 1-8	13	13	13
DIGIT 1-4	14	12	12
DIGIT 1-2	15	11	11
DIGIT 1-1	16	10	10
LOCAL/REMOTE	5	5	5
COMMAND	9	9	9
FLAG	17	7	7
RESET	24	1	1
ERROR	3	3	3
CONTINUITY	1	18	4
CONTINUITY	18	19	6
GROUND	36	20-37	18-24

Figure A-2(d): Corresponding Pin-outs of Connectors J3, AA4, and AA0

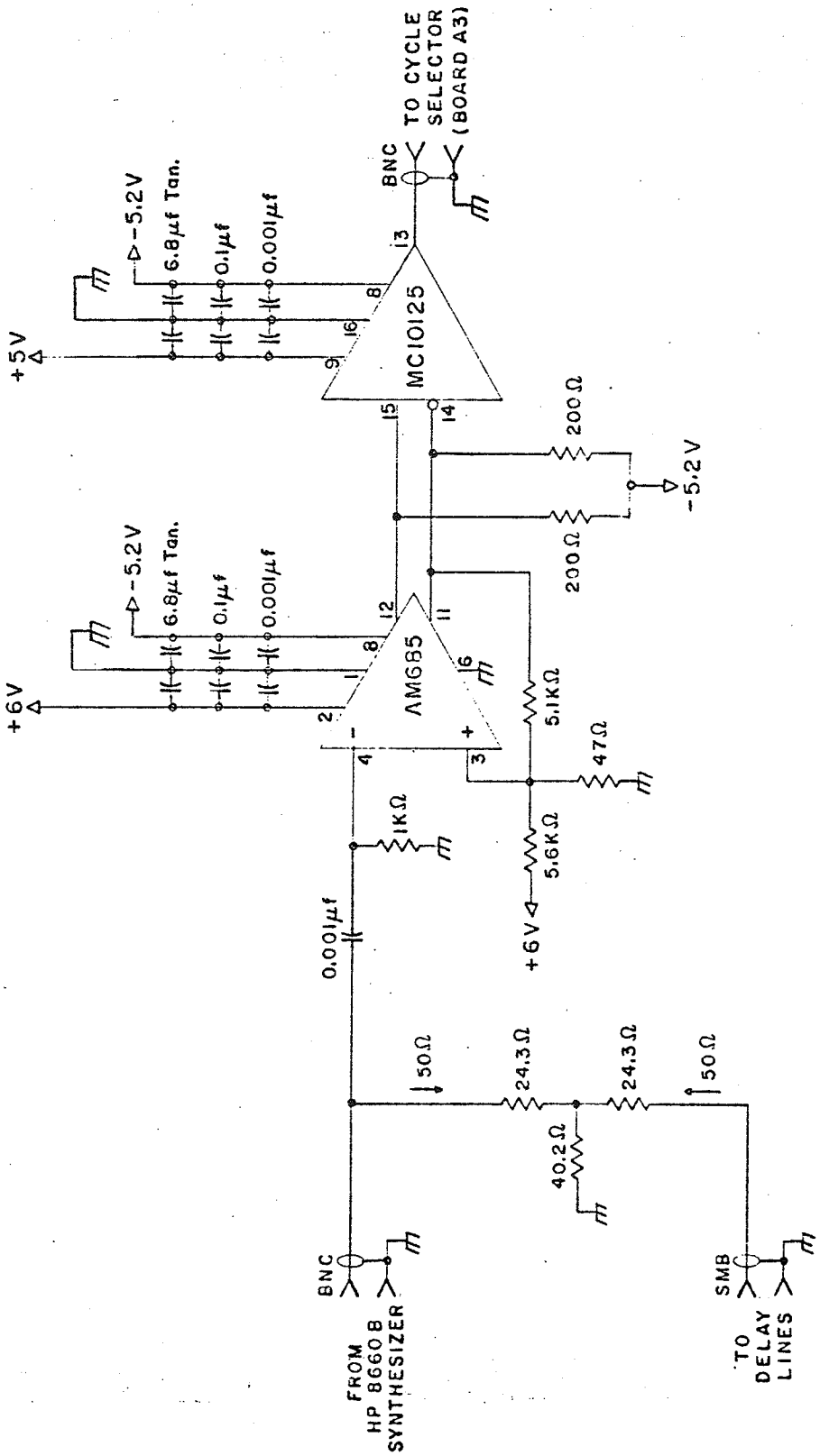


Figure A-3(a): Zero Crossing Detector of the Programmable Window Generator (Board A2)

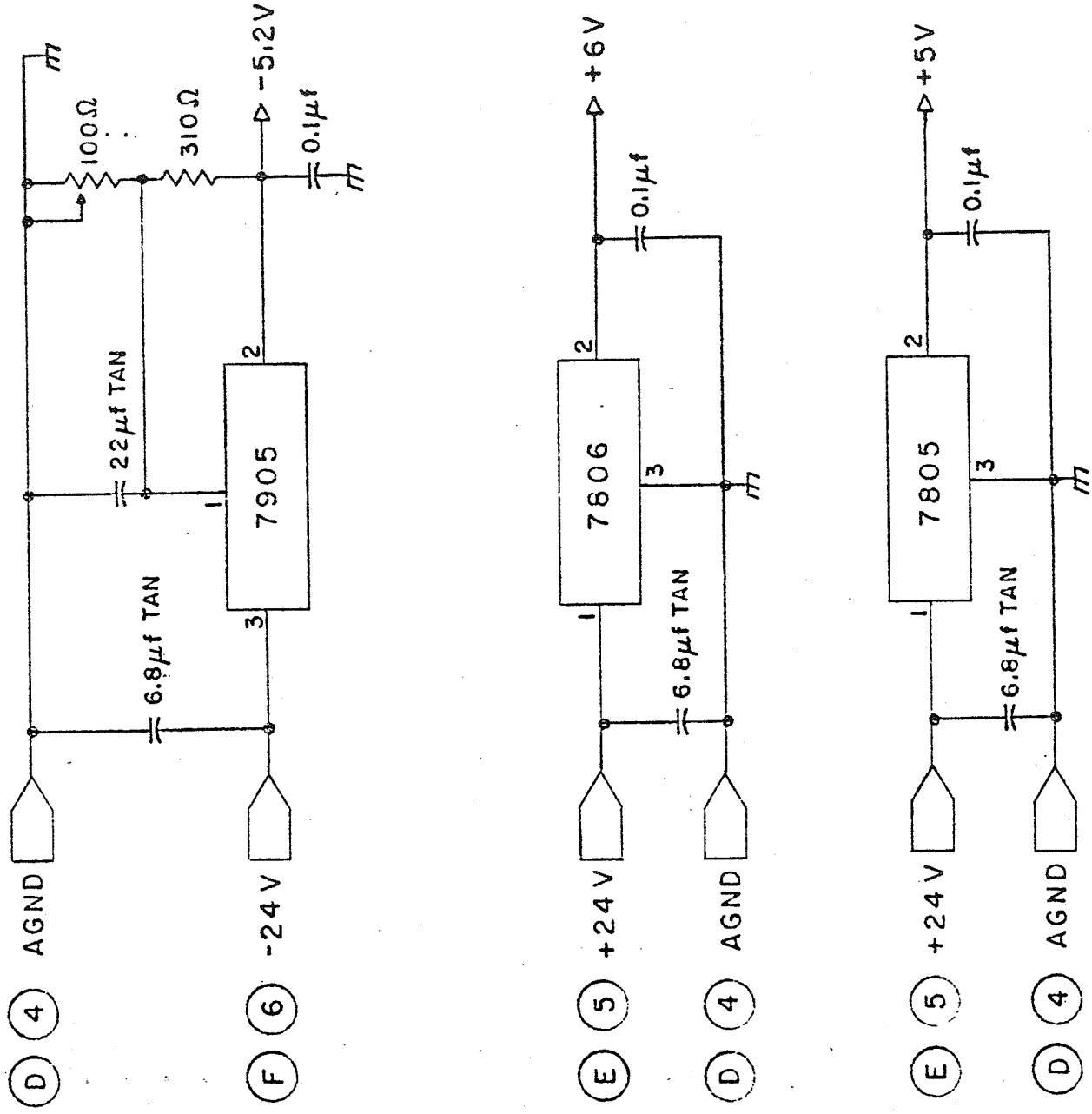


Figure A-3(b): On-board Voltage Regulators for the Zero Crossing Detector of the Programmable Window Generator (Board A2)

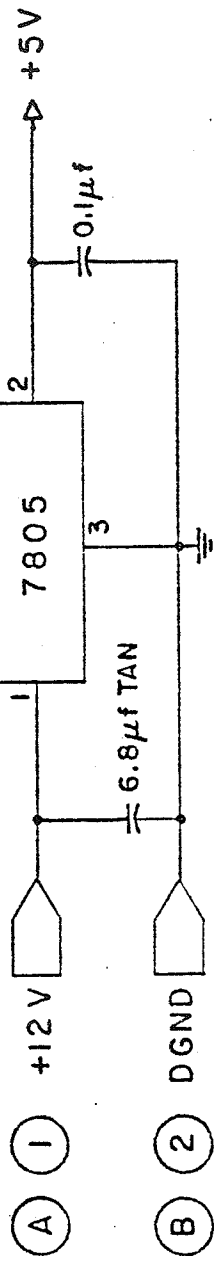


Figure A-3(c): On-board Voltage Regulators for Boards A0, A1, and A3

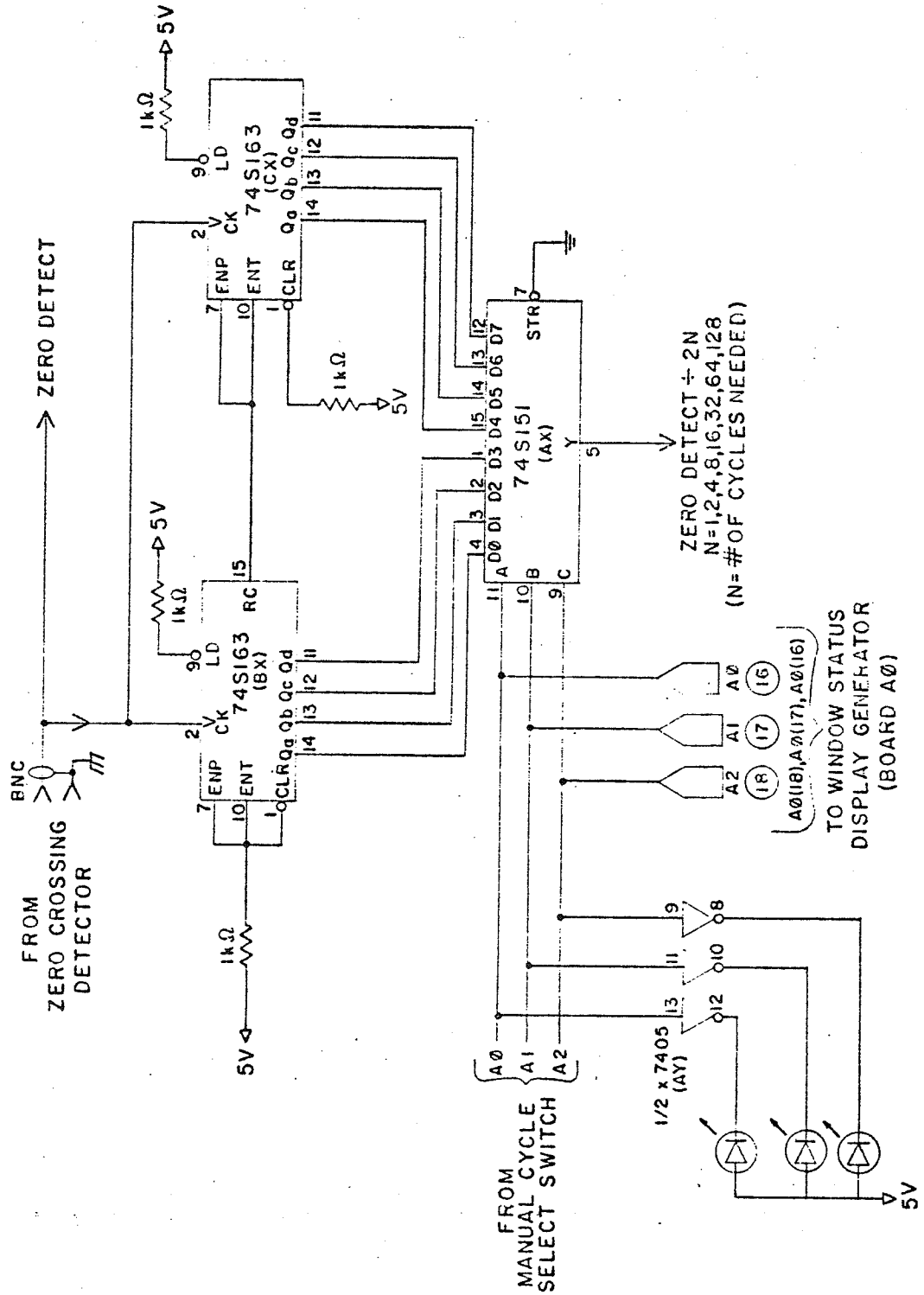
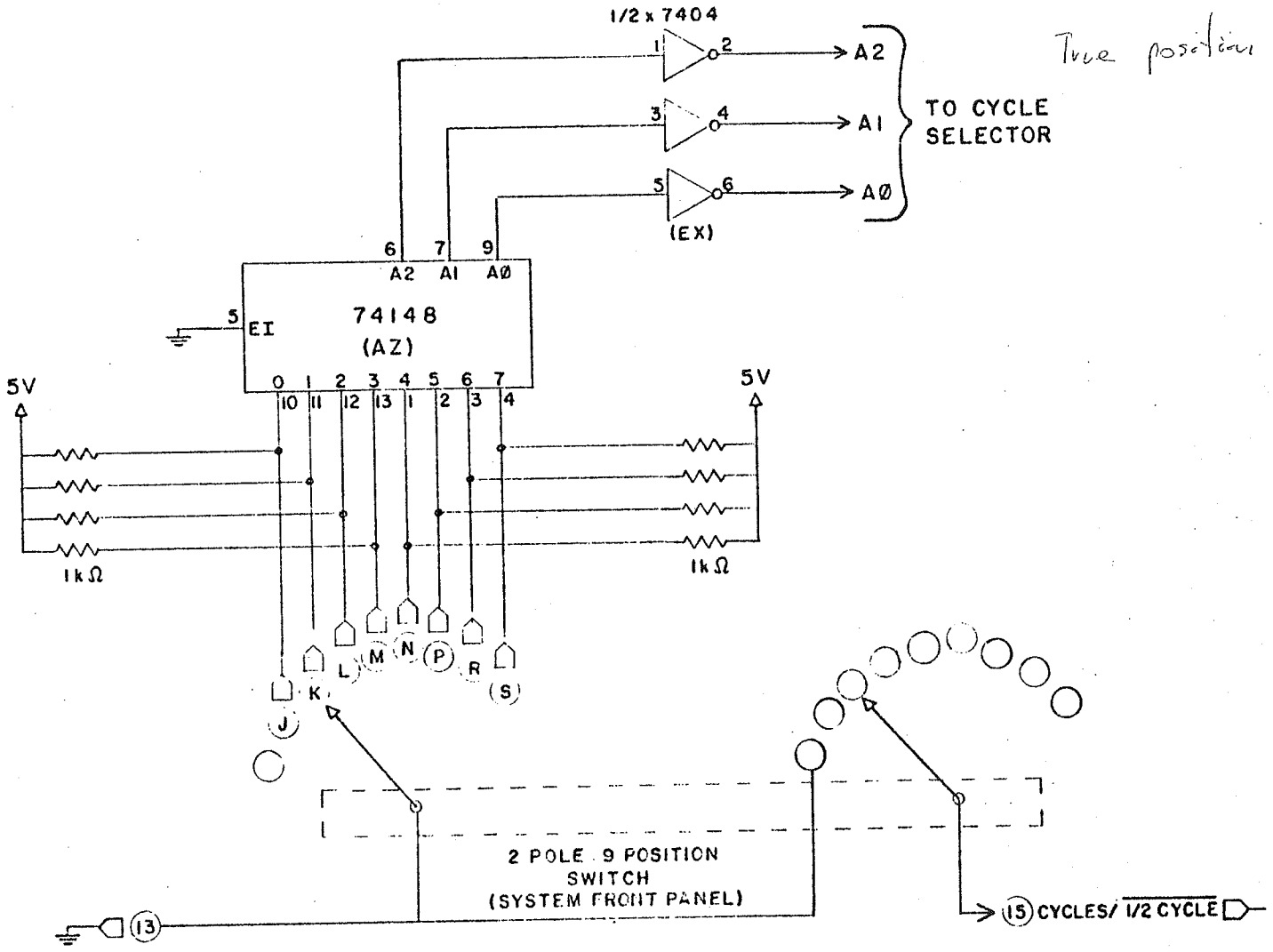


Figure A-3(d): Cycle Selector of the Programmable Window Generator (Board A3)



True position indicators

Figure A-3(e): Manual Cycle Select Switch of the Programmable Window Generator (Board A3)

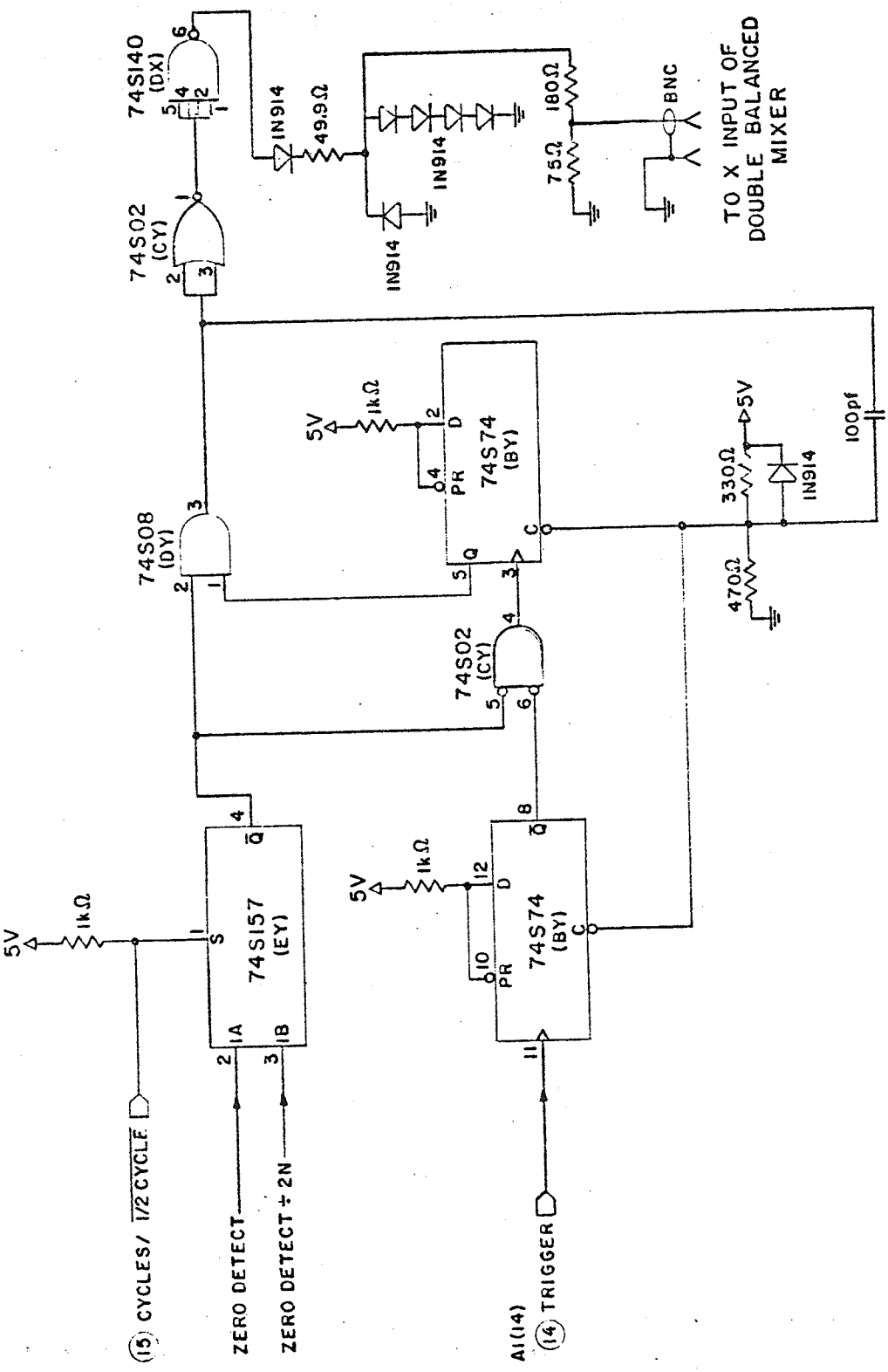


Figure A-3(f): Synchronizer of the Programmable Window Generator (Board A3)

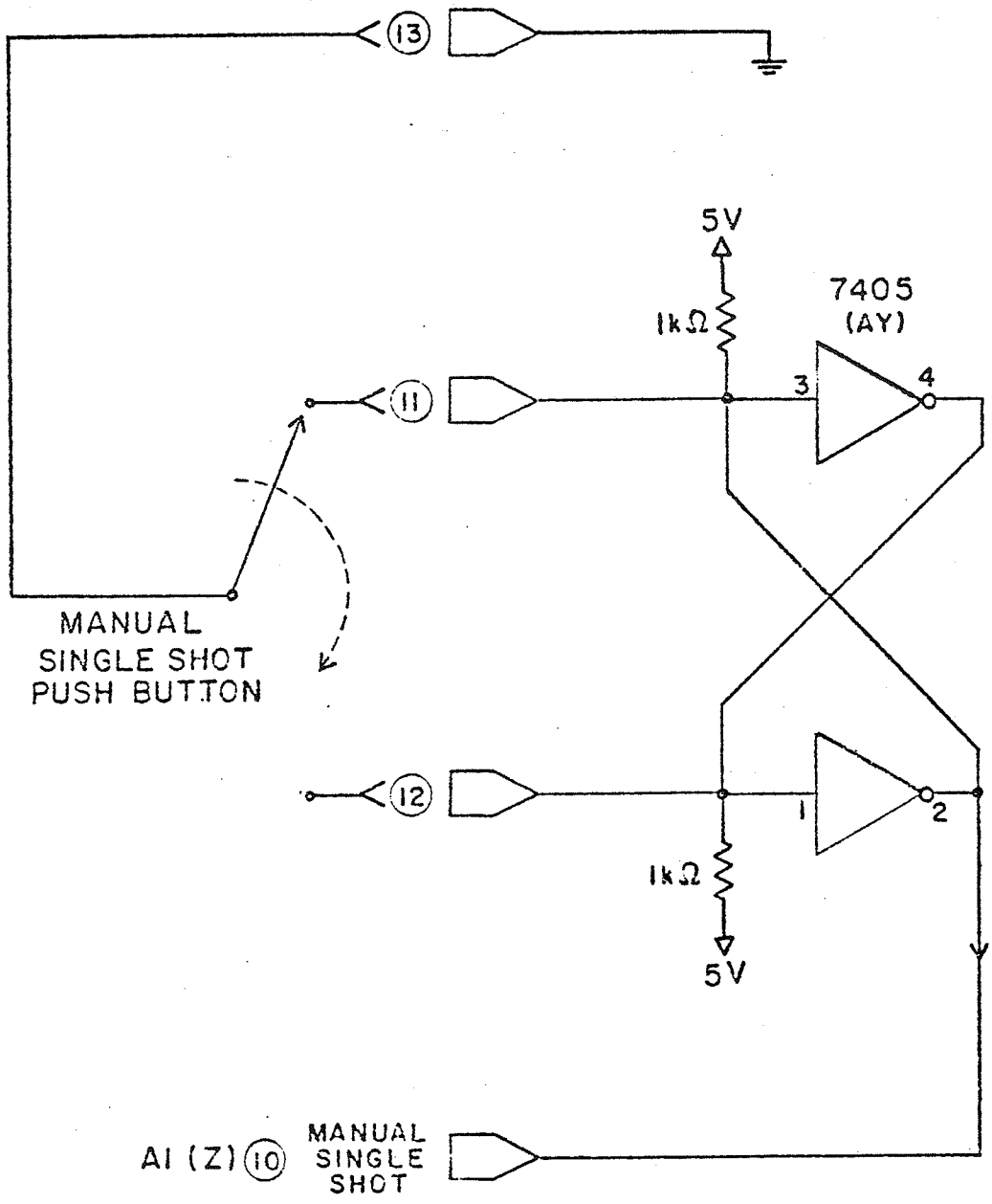


Figure A-3(g): Manual Single Shot Push Button and Debounce Latch of the Programmable Window Generator (Board 3)

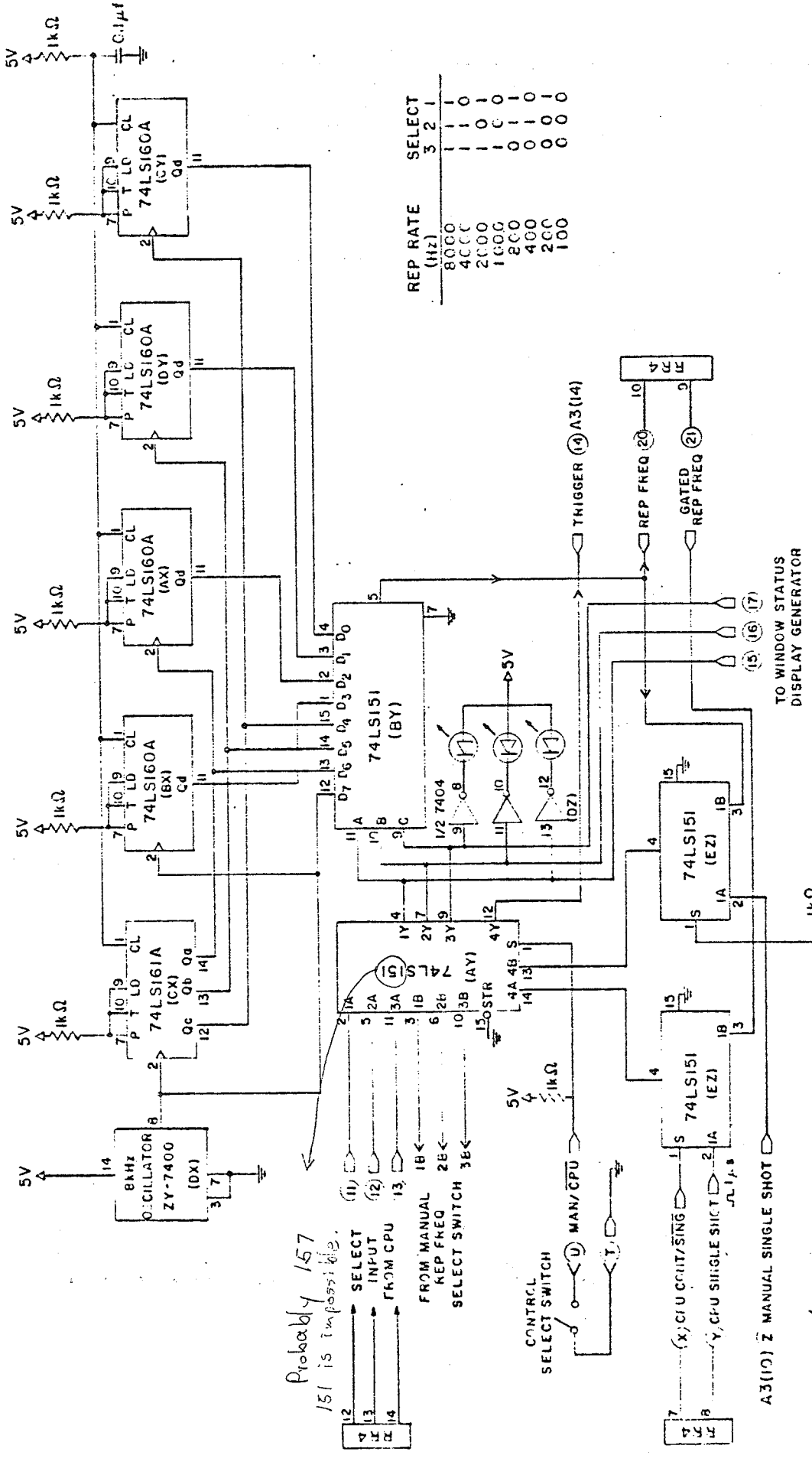


Figure A-3(h): Repitition Frequency Generator and Trigger Control Selection Logic (Board A1)

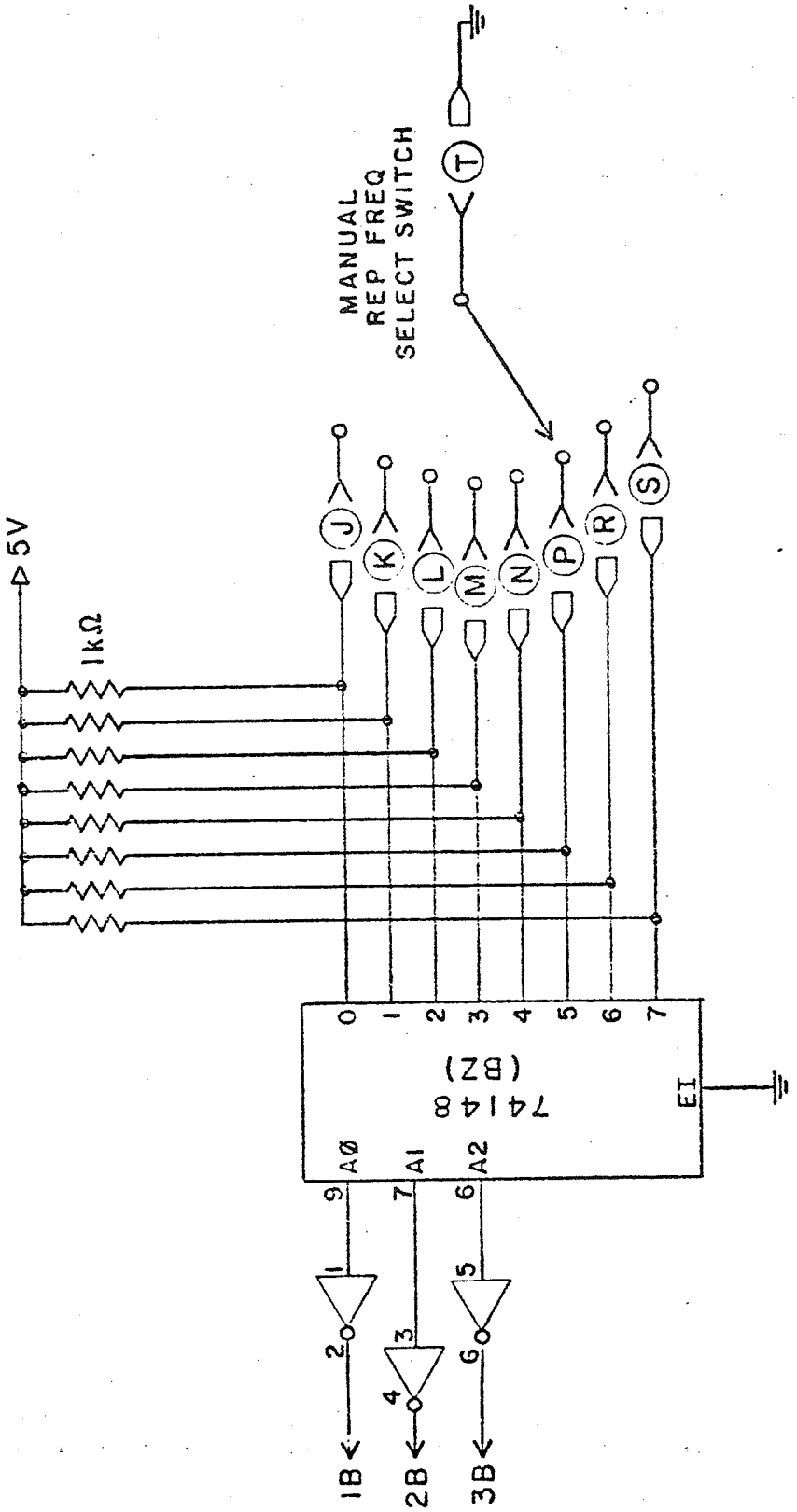


Figure A-3(i): Manual Repitition Frequency Select Switch of the Progammable Window Generator

(Board A1)

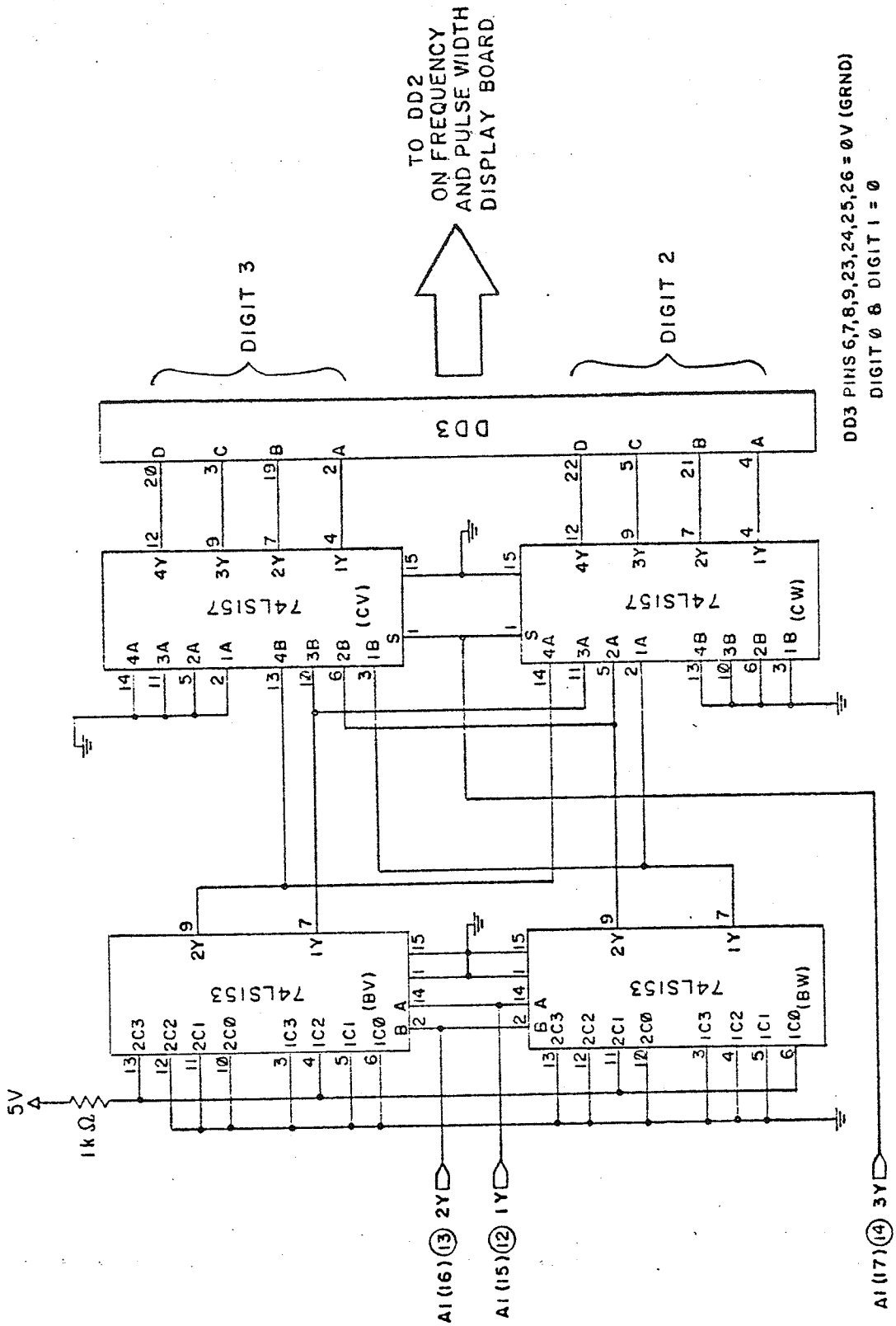


Figure A-3(j): Window Status Display Generator of the Programmable Window Generator
(Pulse Repitition Frequency Display code) (Board A0)

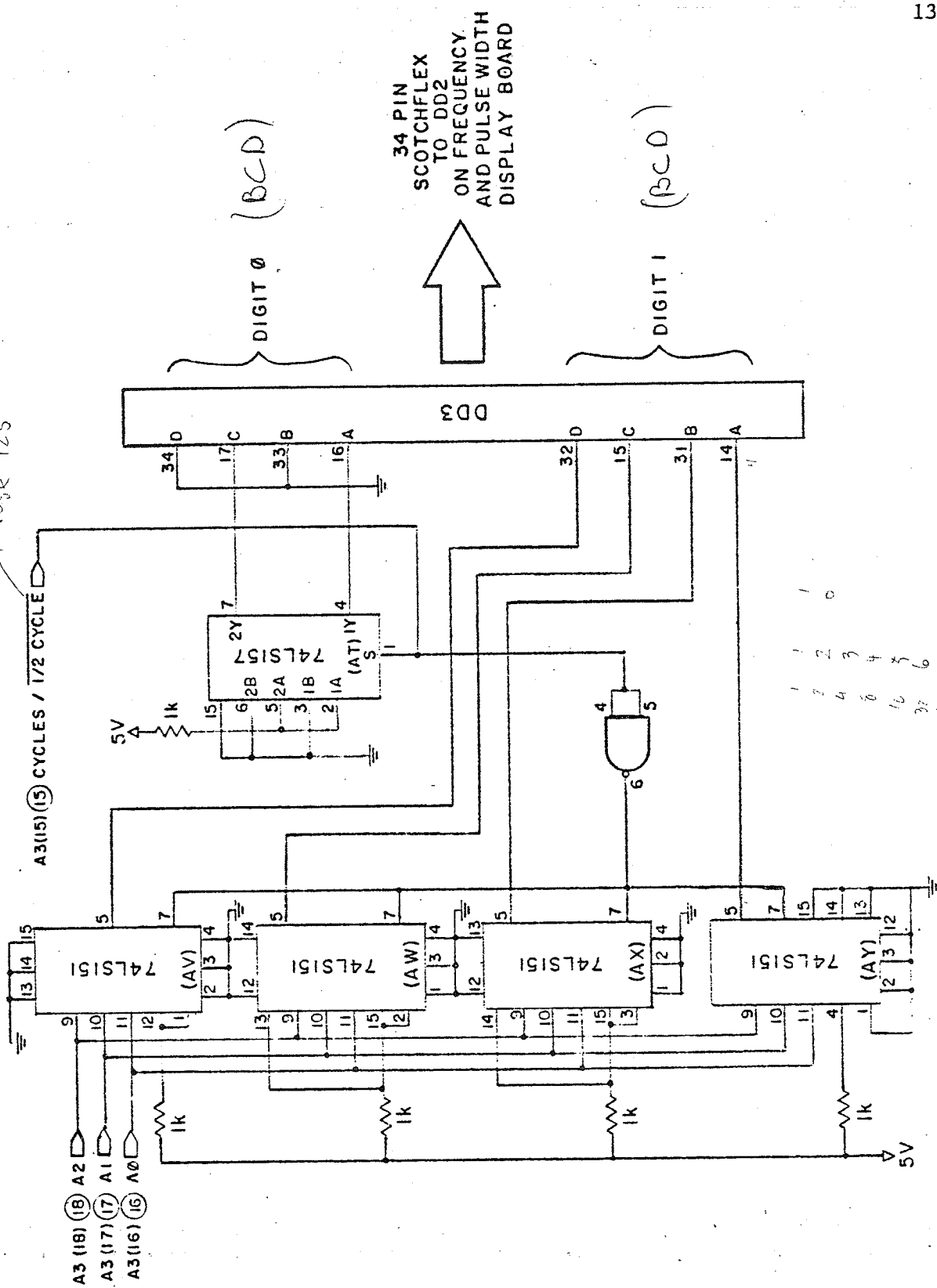


Figure A-3(k): Window Status Display Generator of the Programmable Window Generator (Pulse Width Display Code) (Board A0)

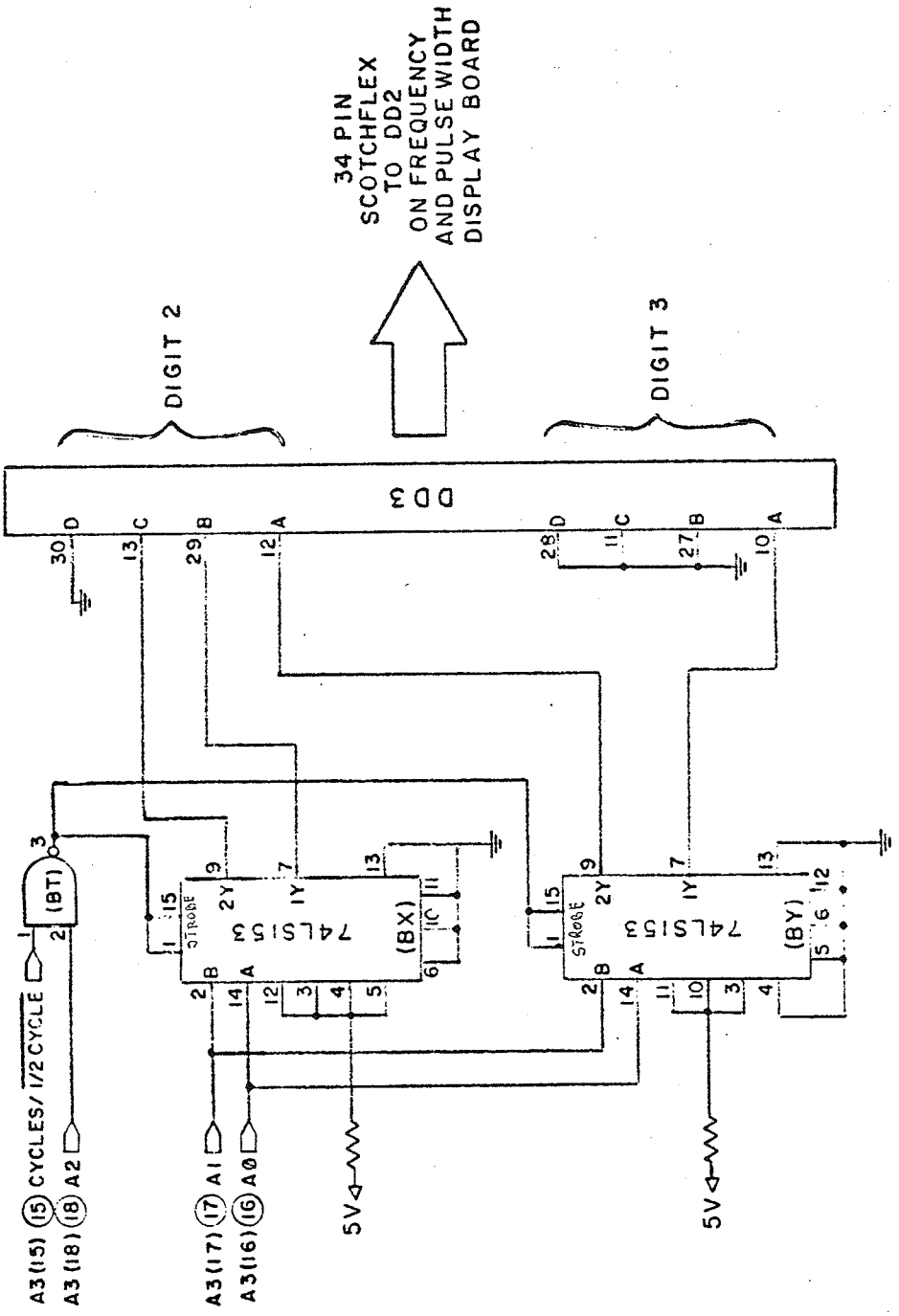


Figure A-3(1): Window Status Display Generator of the Programmable Window Generator

(Pulse Width Display Code) (Board A0)

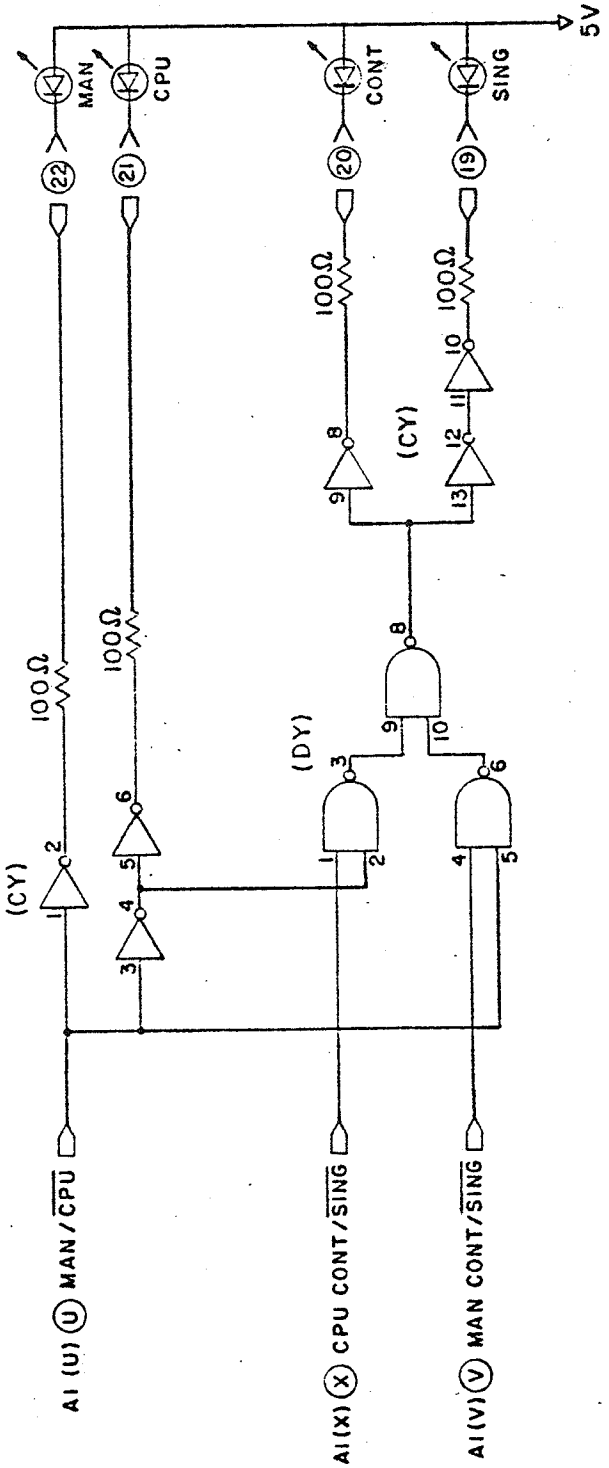


Figure A-3(m): Window Status Display Generator of the Programmable Window Generator (Mode Display) (Board A0)

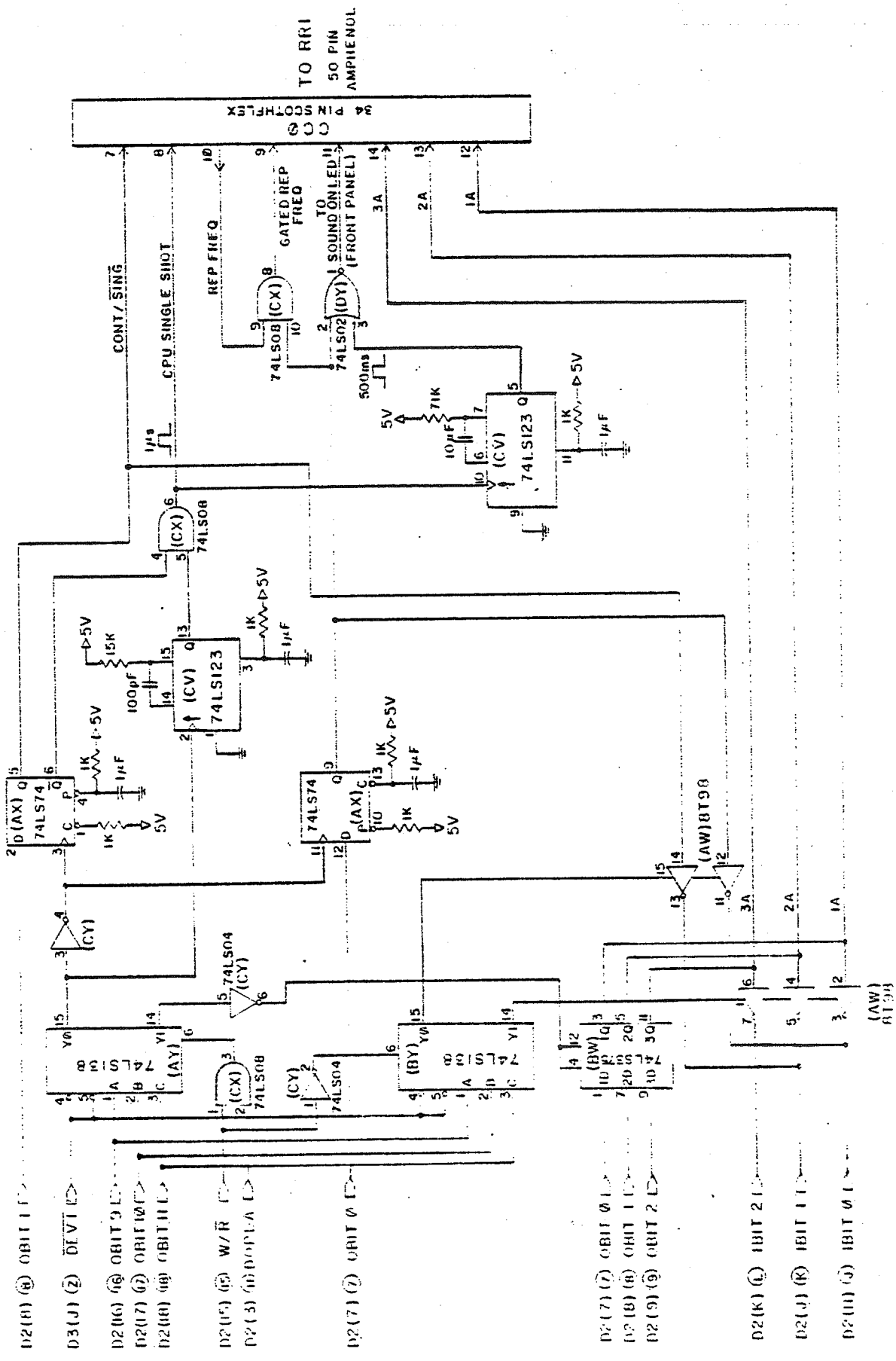


Figure A-4: Programmable Window Generator Controller (Device 1) (Board D5)

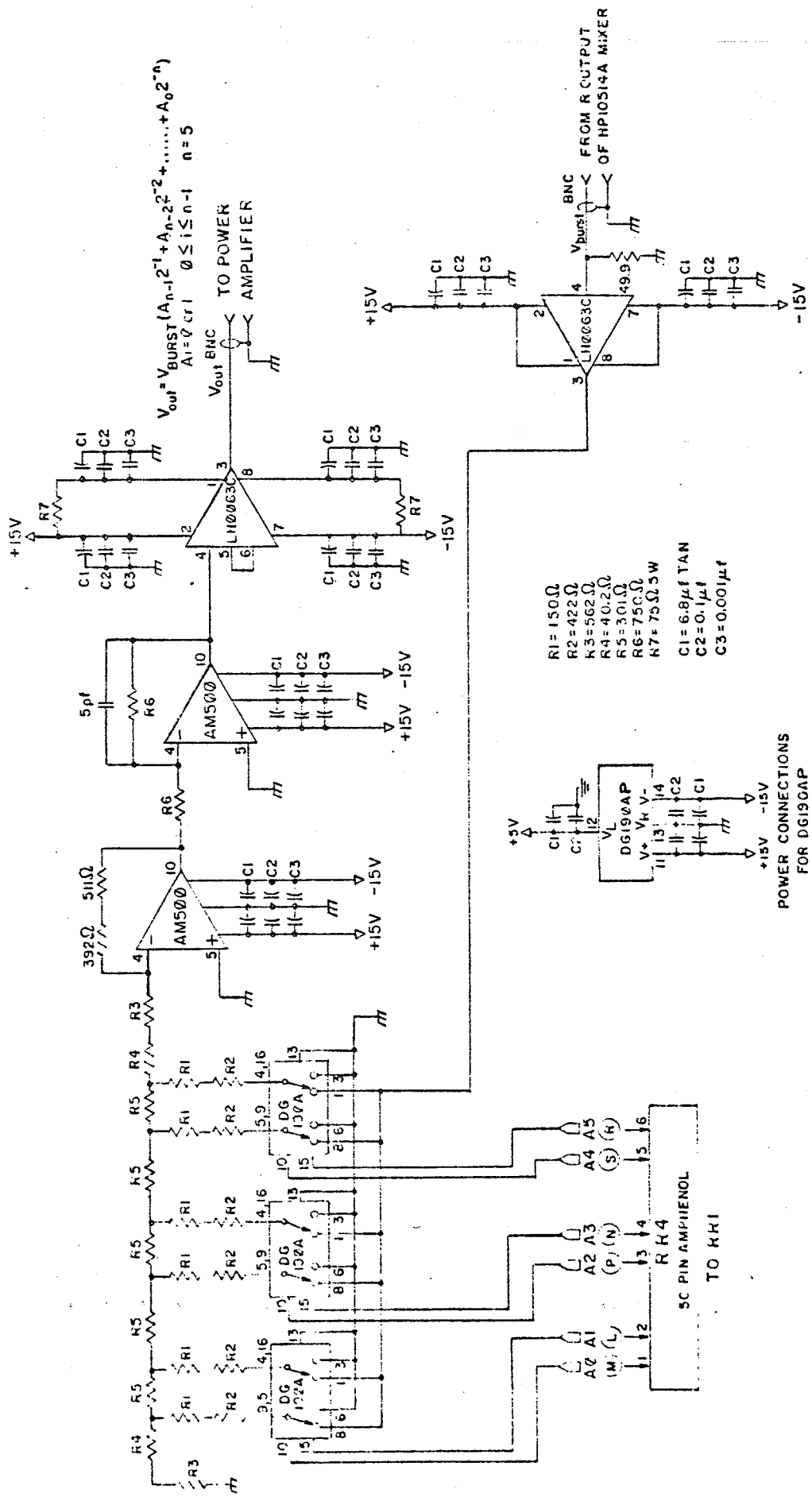


Figure A-5: Programmable Attenuator and Buffer Amplifier

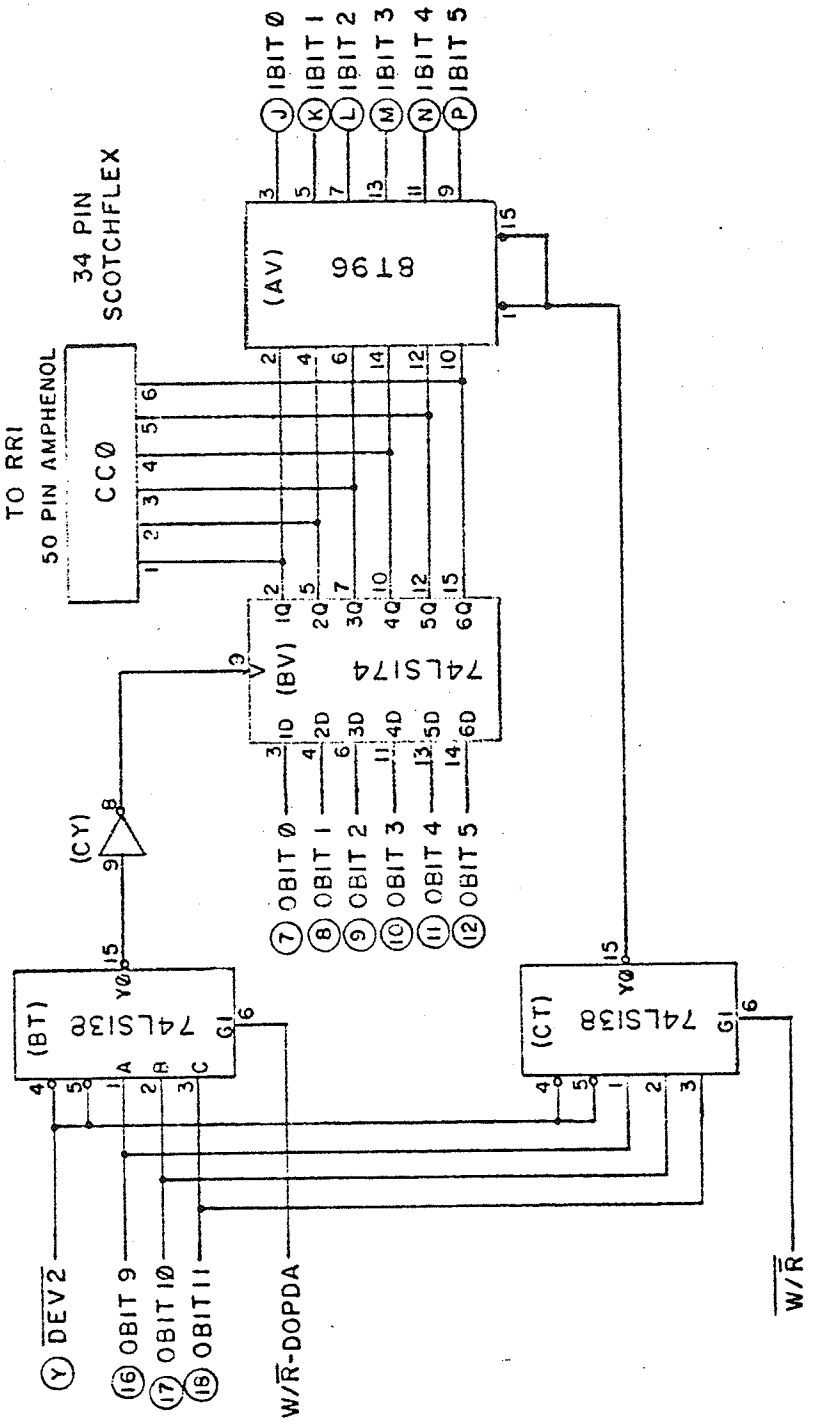


Figure A-6: Programmable Attenuator Controller (Device 2) (Board D5)

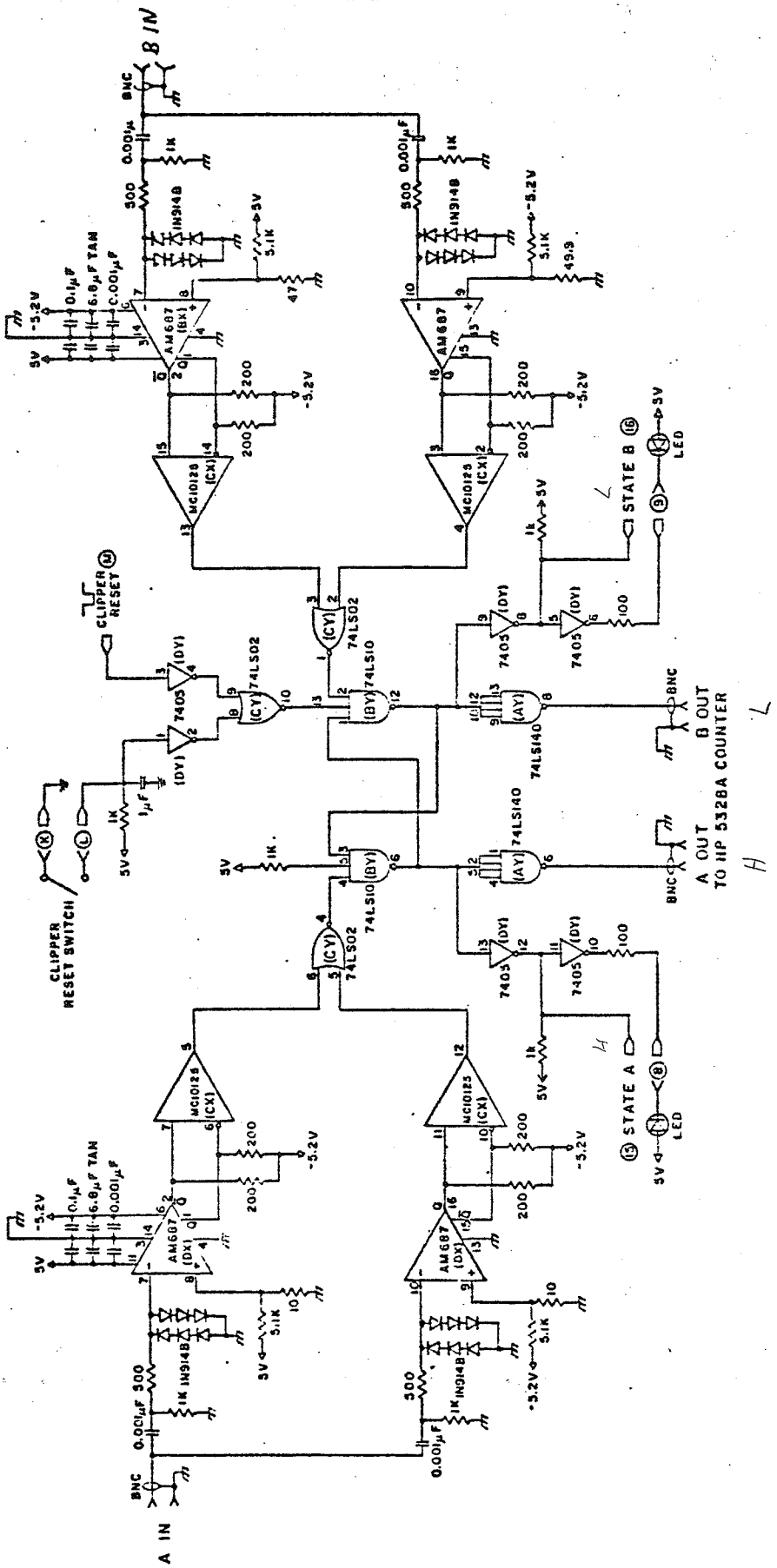


Figure A-7(a): The Clipper (Board A4)

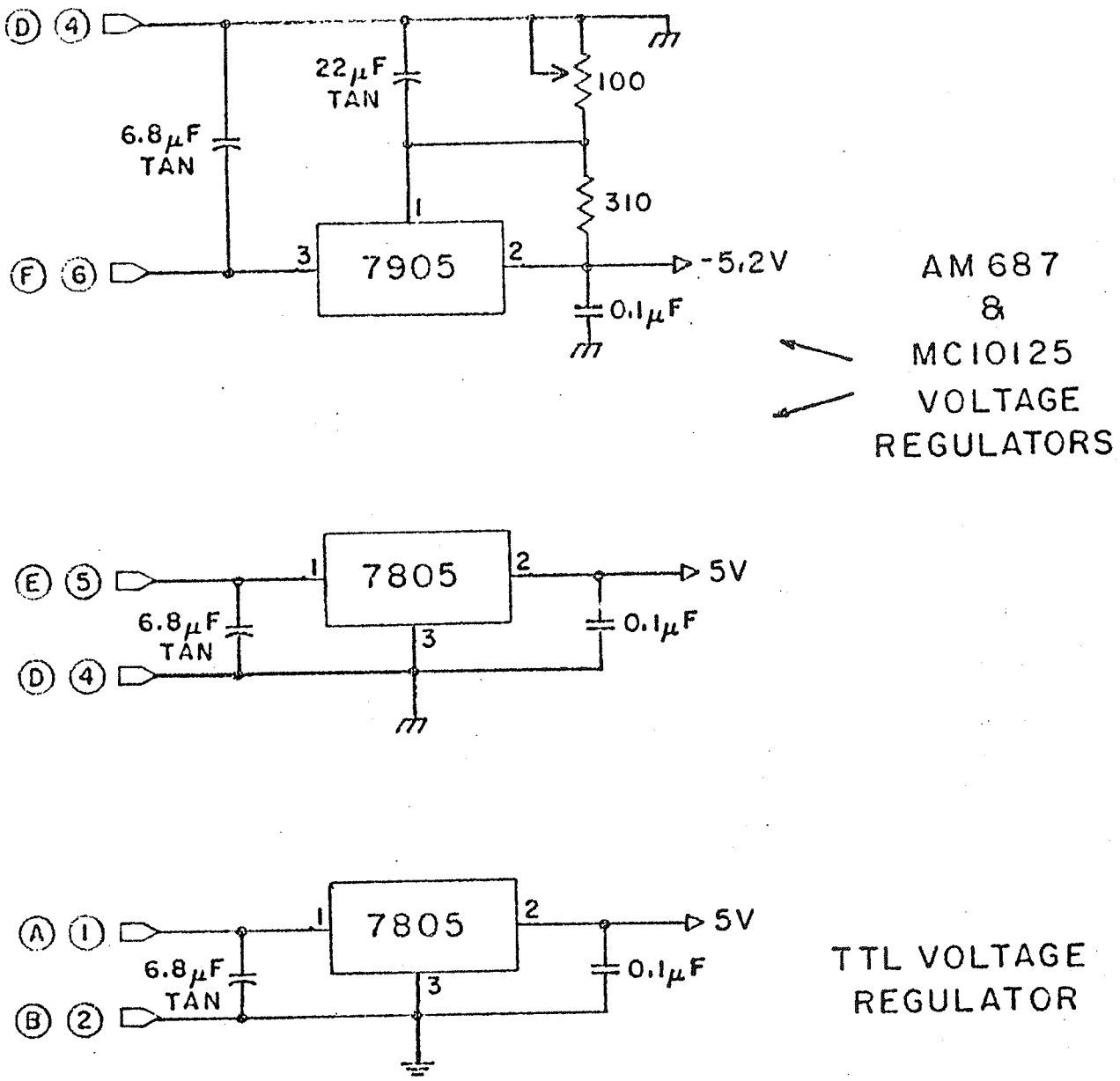


Figure A-7(b): On-board Voltage Regulators for the Clipper (Board A4)

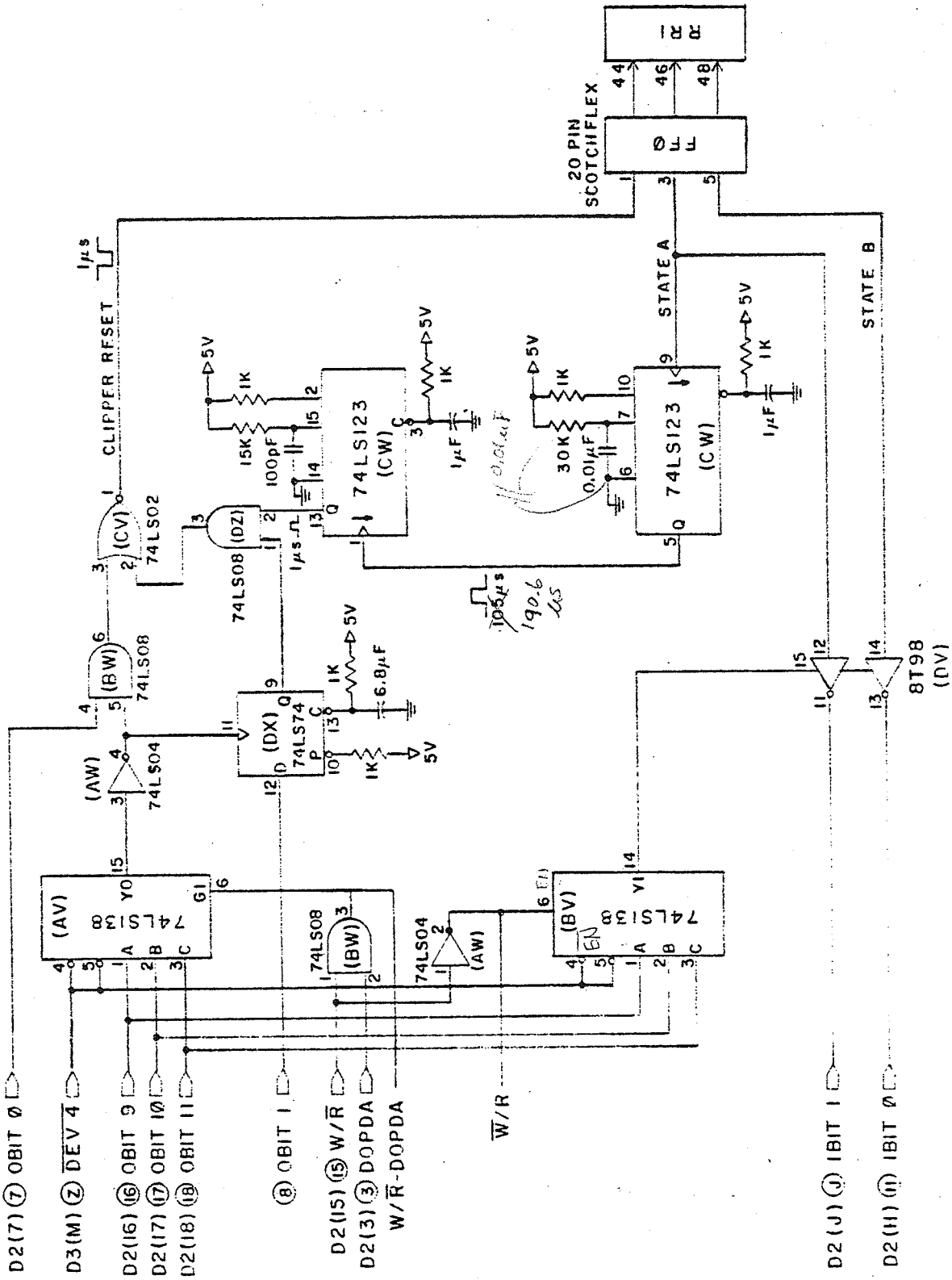


Figure A-8: Clipper Controller (Device 4) (Board D8)

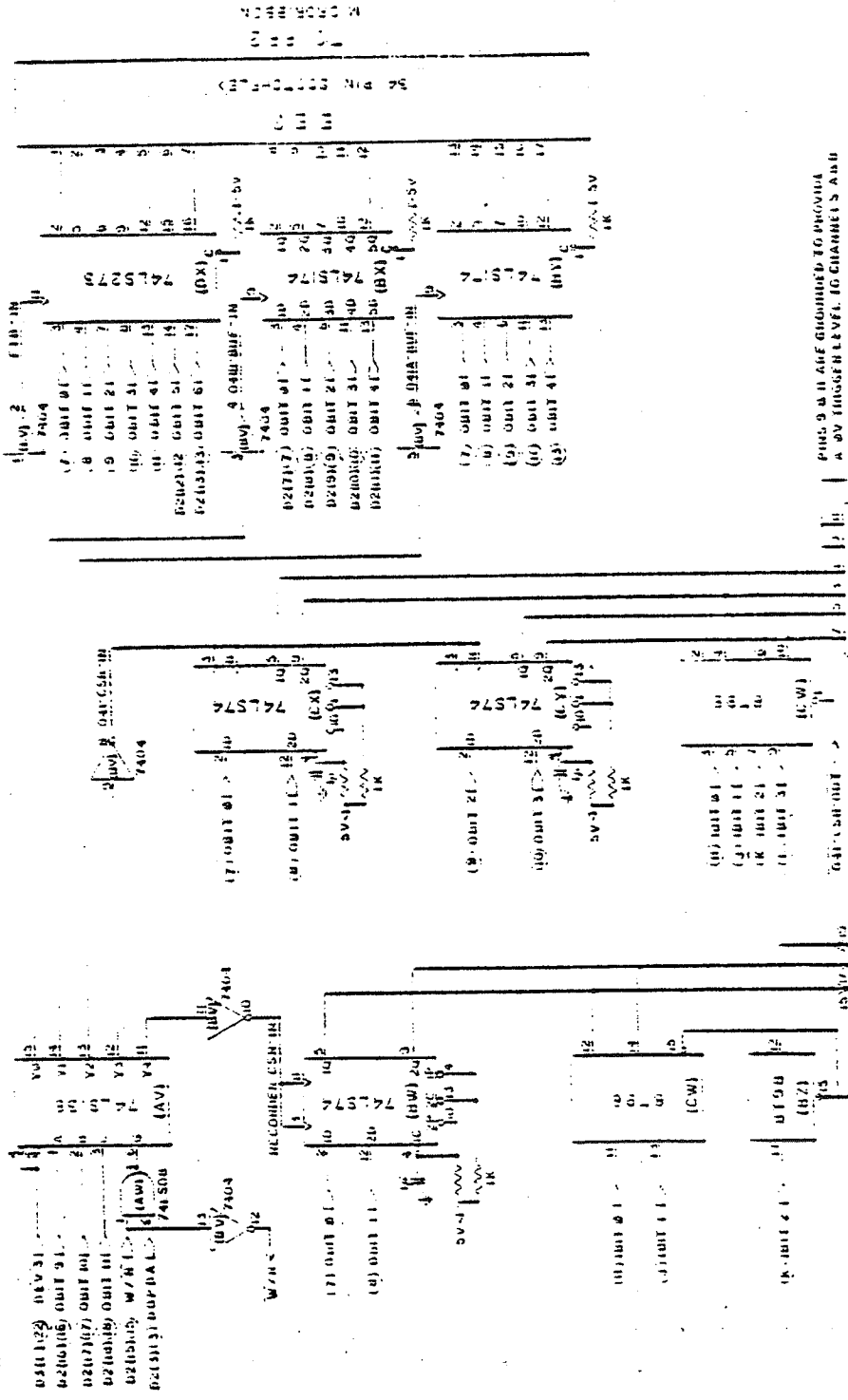


Figure A-9(a): HP 5328A Counter Controller (Device 3) (Board 17)

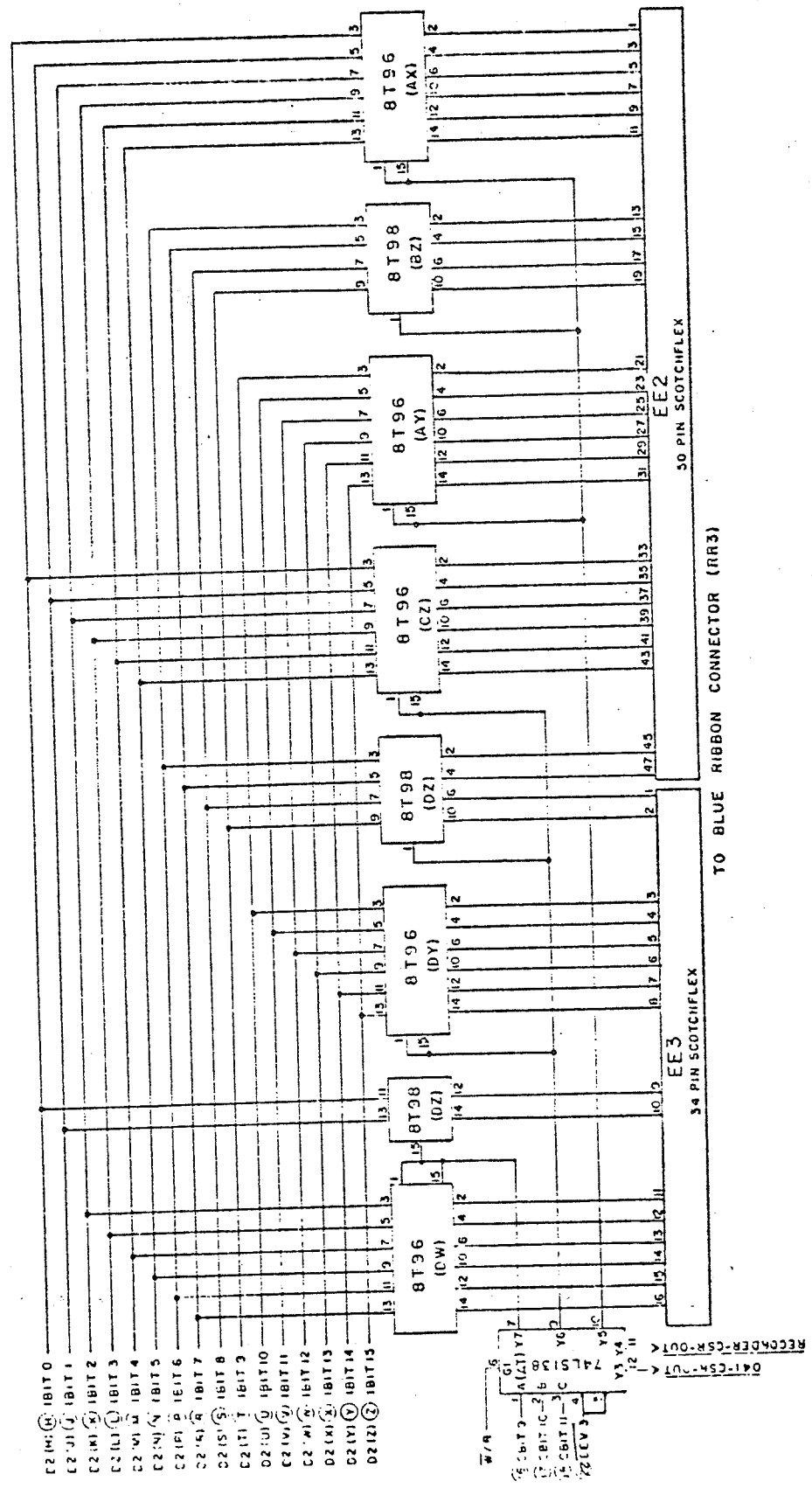


Figure A-9(b): HP 5328A Counter Controller (Device 3) (Board D7)

34 PIN SCOTCHFLEX (EEO)	TO MICRO RIBBON (RR2)	
1	14	$\overline{FD}$
2	13	$\overline{FC}$
3	2	$\overline{FB}$
4	1	$\overline{FA}$
5	16	$\overline{TBC}$
6	15	$\overline{TBB}$
7	3	$\overline{TBA}$
8	7	Impedance B
9	8	Coupling B
10	9	Slope B
11	10	Attenuator B
12	11	Invert-Normal
13	19	Impedance A
14	20	Coupling A
15	21	Slope A
16	22	Attenuator A
17	23	Sep-com A

* Note: Connectors RR2 and RR3 has the same pin designation as the REMOTE PROGRAMMING and RECORDER OUTPUT connectors at the back of the HP 5328A counter. RR2 and RR3 are connected to the REMOTE PROGRAMMING and RECORDER OUTPUT Connectors respectively via two cables.

Figure A-9(c): Connector Pin Designations for the HP 5328A Counter Controller (Board D7)

20 PIN SCOTCHFLEX (EE1)		TO MICRO RIBBON (RR2)	
1		4	LRPR
3		5	RLEXT
5		6	RLRES
7		18	Data Valid
9	GND	24	LEVEL A
11	GND	12	LEVEL B

	BLUE RIBBON (RR3)	
15	22	+ve inhibit
17	47	-ve inhibit
19	48	Neg-print Command

Figure A-9(d): Connector Pin Designations for the HP 5328A Counter Controller (Board D7)

50 PIN SCOTCHFLEX (EE2)		TO BLUE RIBBON (RR3)	
1	1	A	
3	2	B	COL 1
5	26	C	10^0
7	27	D	
9	3	A	
11	4	B	COL 2
13	28	C	10^1
15	29	D	
17	5	A	
19	6	B	COL 3
21	30	C	10^2
23	31	D	
25	7	A	
27	8	B	COL 4
29	32	C	10^3
31	33	D	
33	9	A	
35	10	B	COL 5
37	34	C	10^4
39	35	D	
41	11	A	
43	12	B	COL 6
45	36	C	10^5
47	37	D	

Figure A-9(e): Connector Pin Designations for the HP 5328A Counter Controller (Board D7)

34 PIN SCOTCHFLEX (EE3)	TO	BLUE RIBBON (RR3)		
1		13	A	
2		14	B	COL 7
3		38	C	10^6
4		39	D	
5		15	A	
6		16	B	COL 8
7		40	C	10^7
8		41	D	
9		17	A	
10		18	B	COL 9
11		42	C	10^8
12		43	D	
13		19	A	Polarity
14		20	B	and
15		44	C	overflow
16		45	D	out
17		25		+5V HI REF

Figure A-9(f): Connector Pin Designations for the HP 5328A Counter Controller (Board D 7)

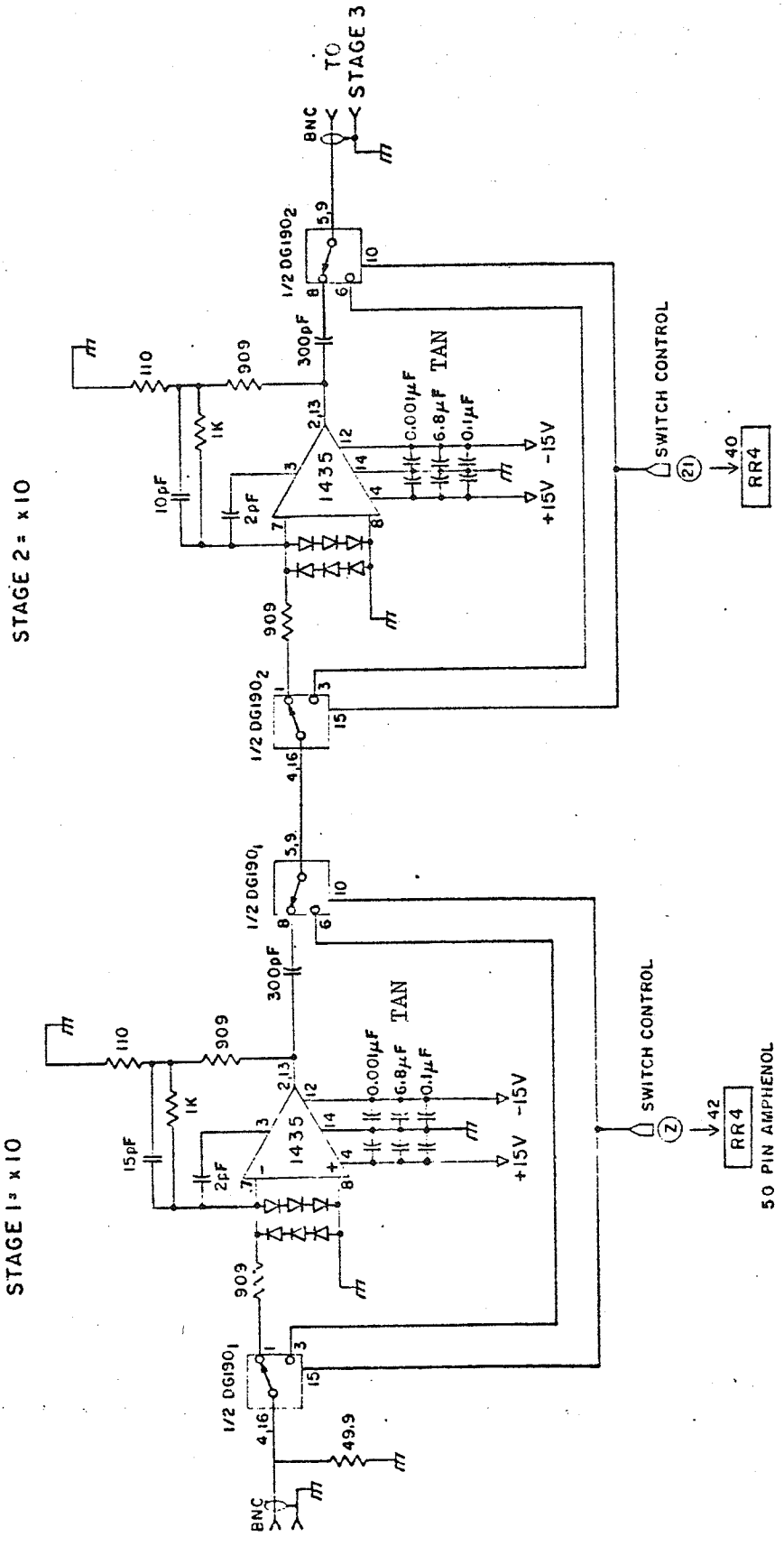


Figure A-10(a): Stages 1 and 2 of Programmable Gain Amplifier (Device 5) (Board A7)

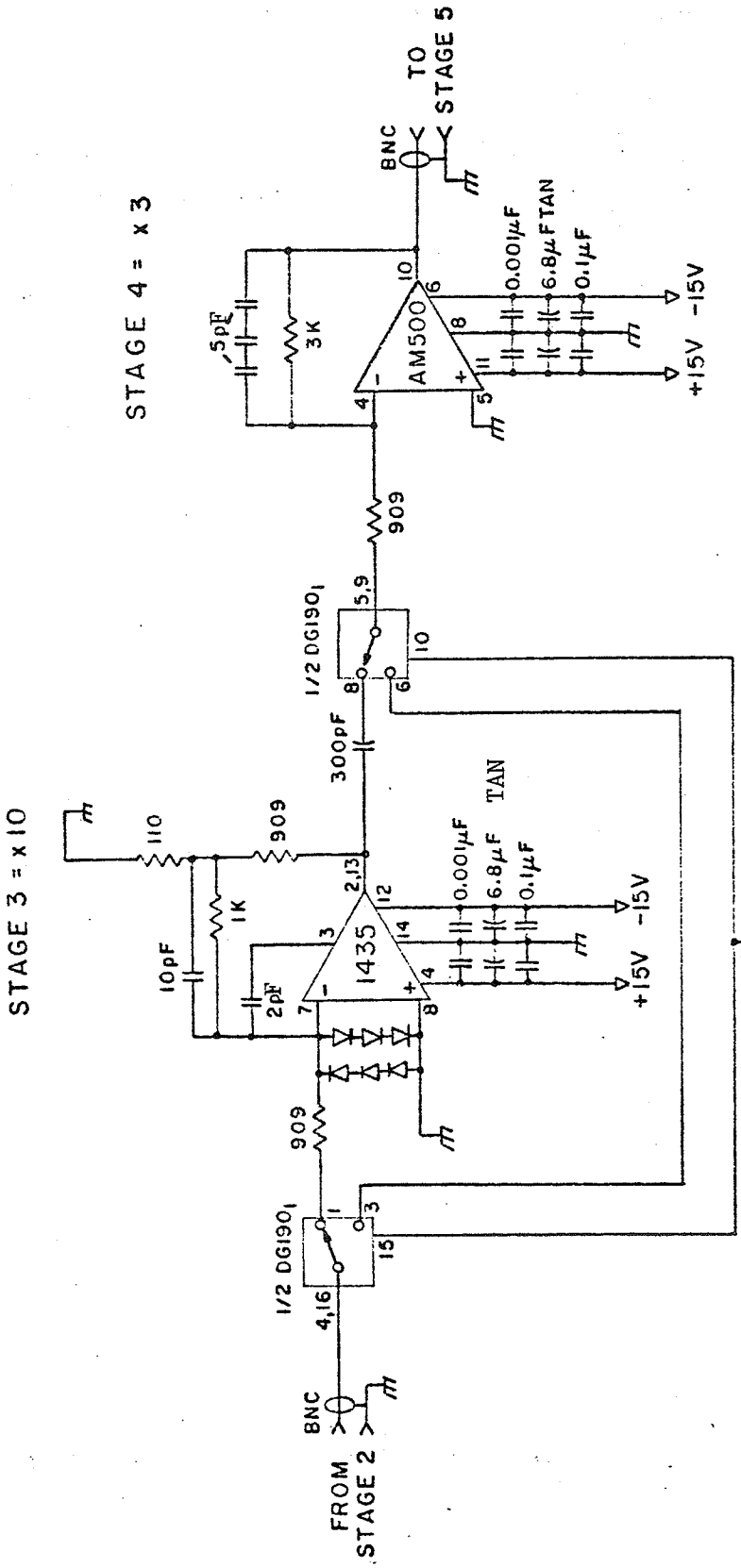


Figure A-10(b): Stages 3 and 4 of Programmable Gain Amplifier (Device 5) (Board A9)

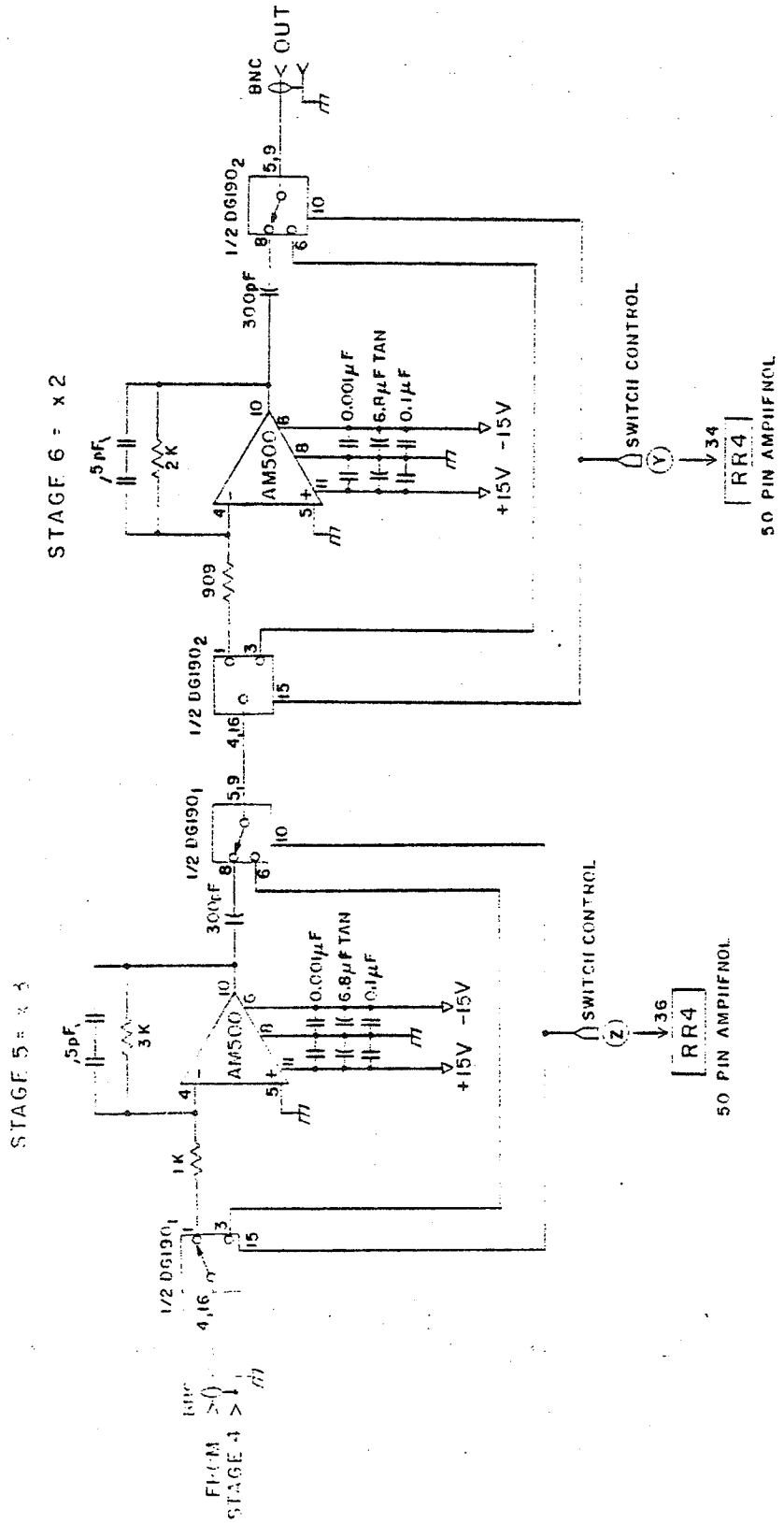


Figure A-10(c): Stages 5 and 6 of Programmable Gain Amplifier (Device 5) (Board A11)

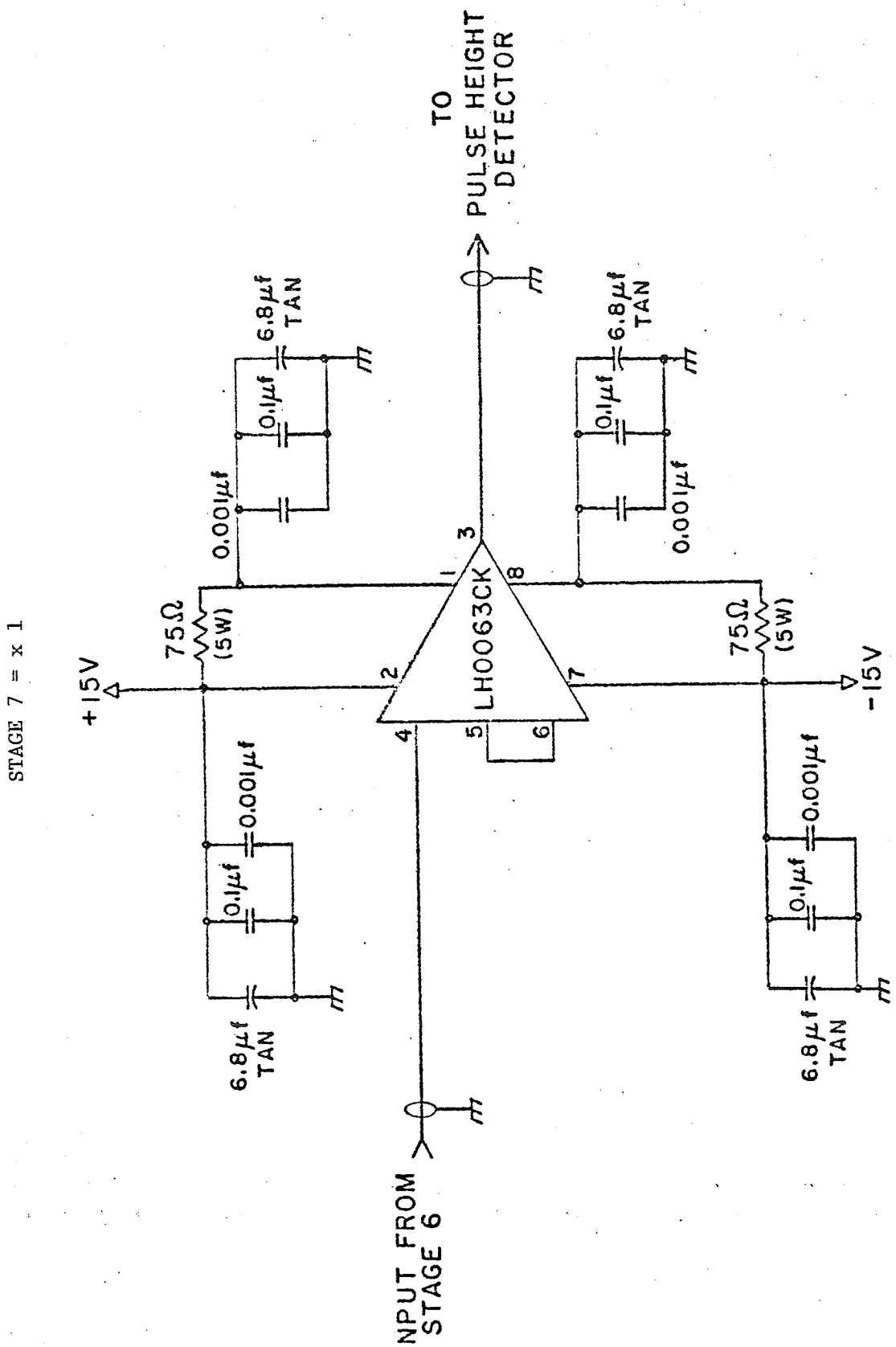


Figure A-10(d): Stage 7 of Programmable Gain Amplifier (Device 5) (Board A12)

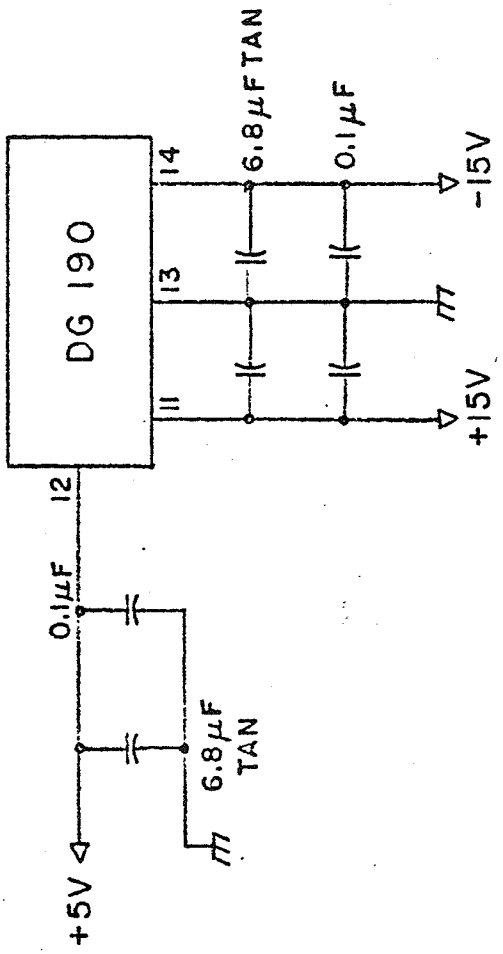


Figure A-10(e): Analog Switch Power Connections of the Programmable Gain Amplifier (Boards A7, A9, and A11)

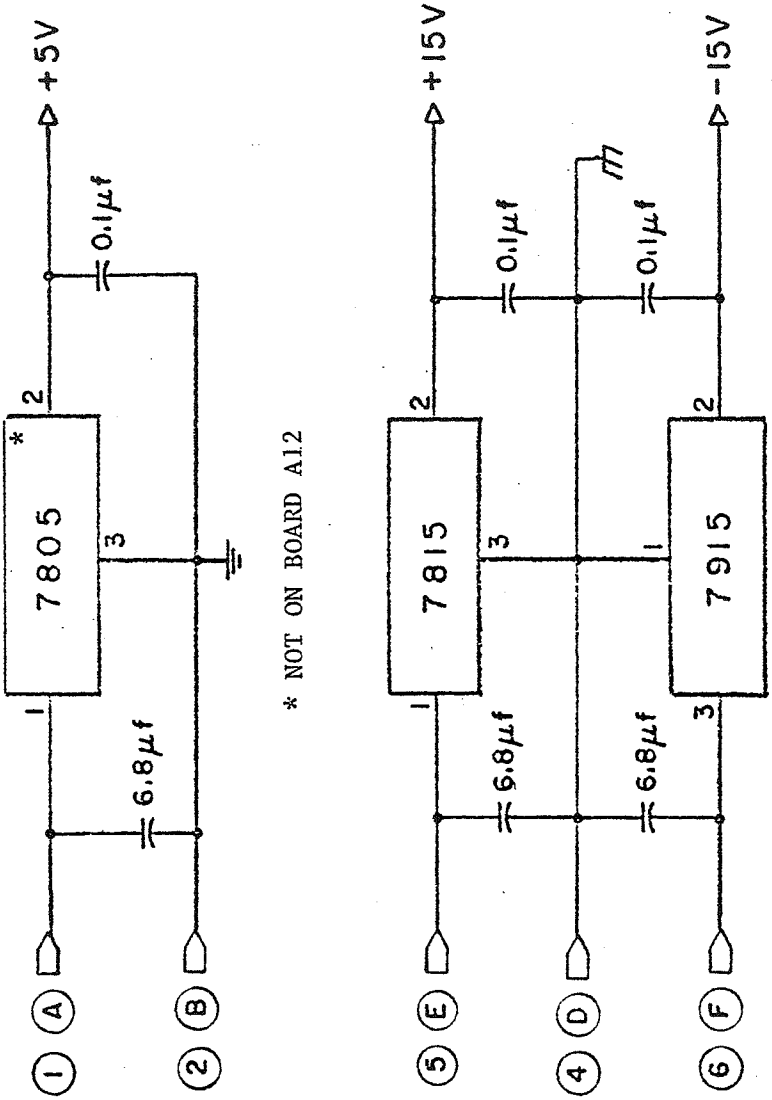


Figure A-10(f): On-board Voltage Regulators of the Programmable Gain Amplifier (Boards A7, A9, A11, and A12).

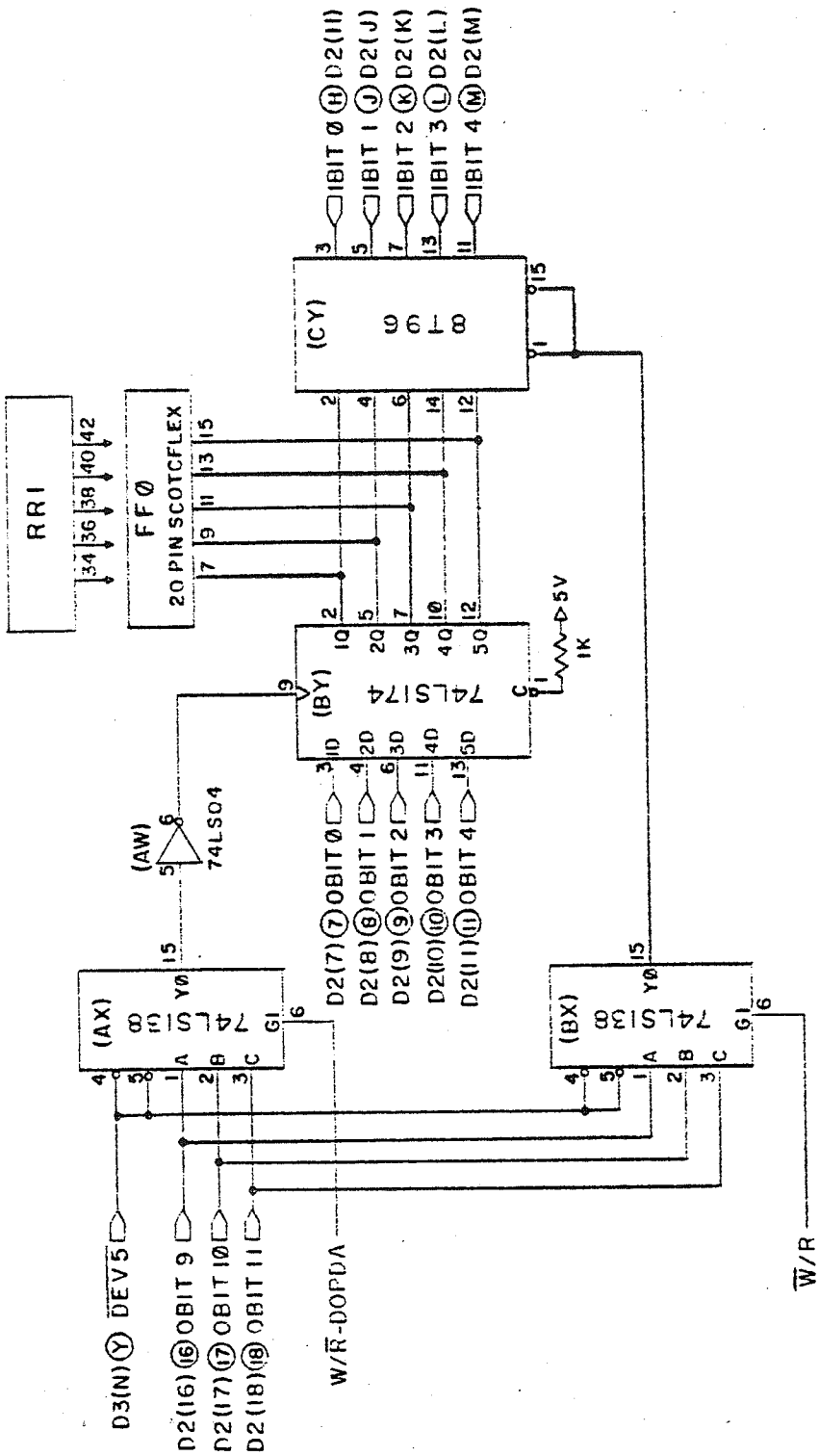


Figure A-11: Programmable Gain Amplifier Controller (Device 5) (Board D8)

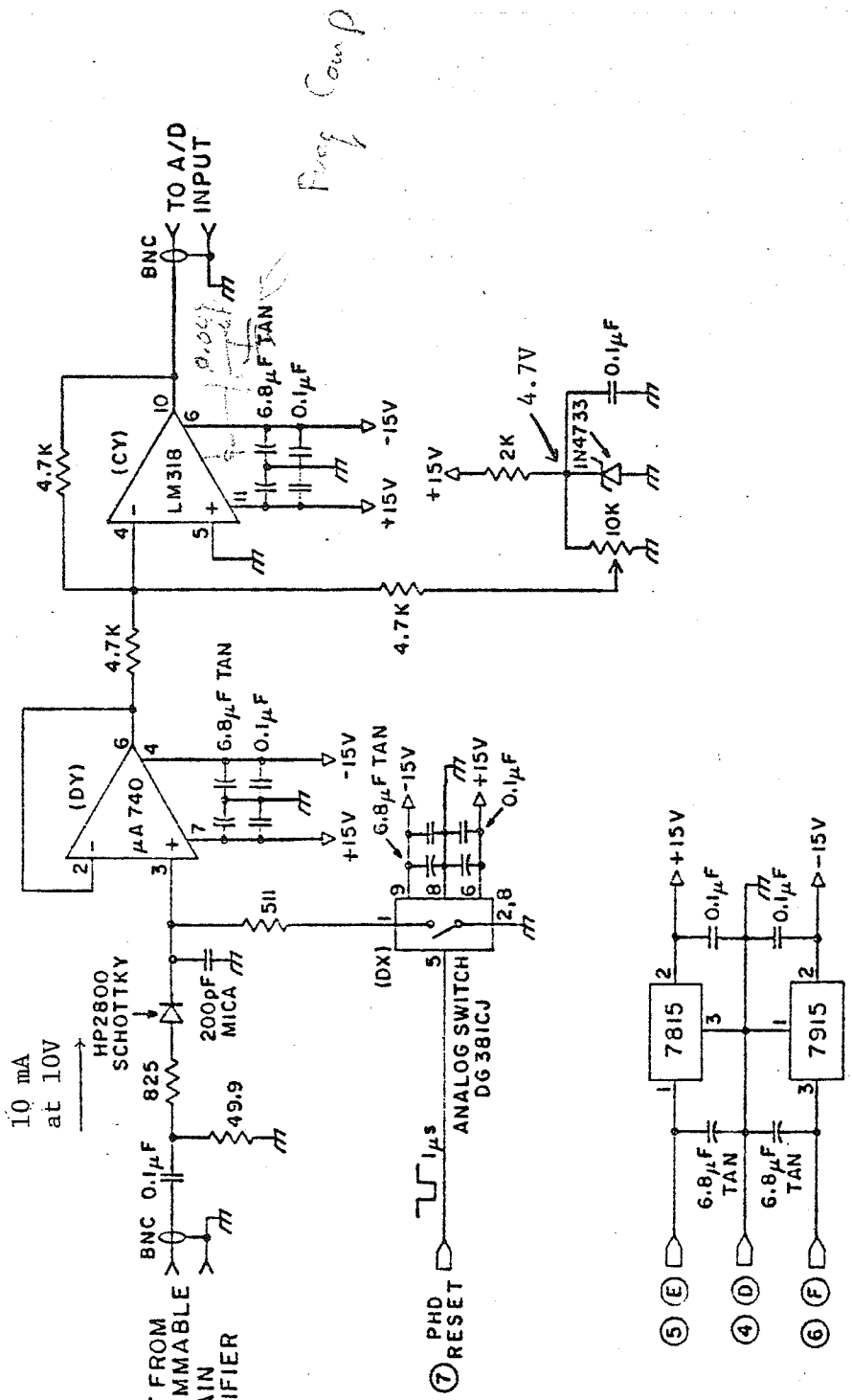


Figure A-12: Pulse Height Detector (Device 6) (Board A 13)

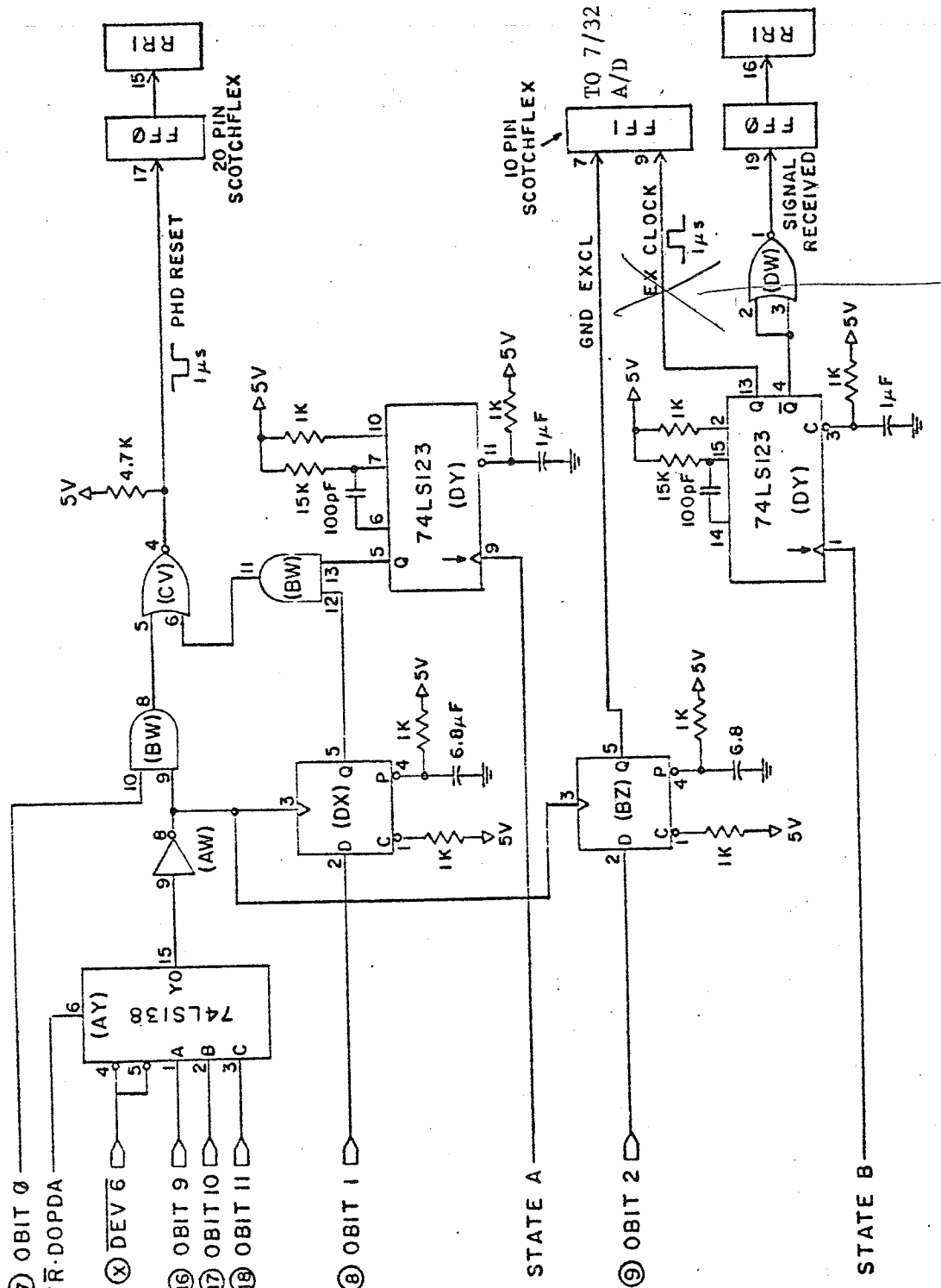
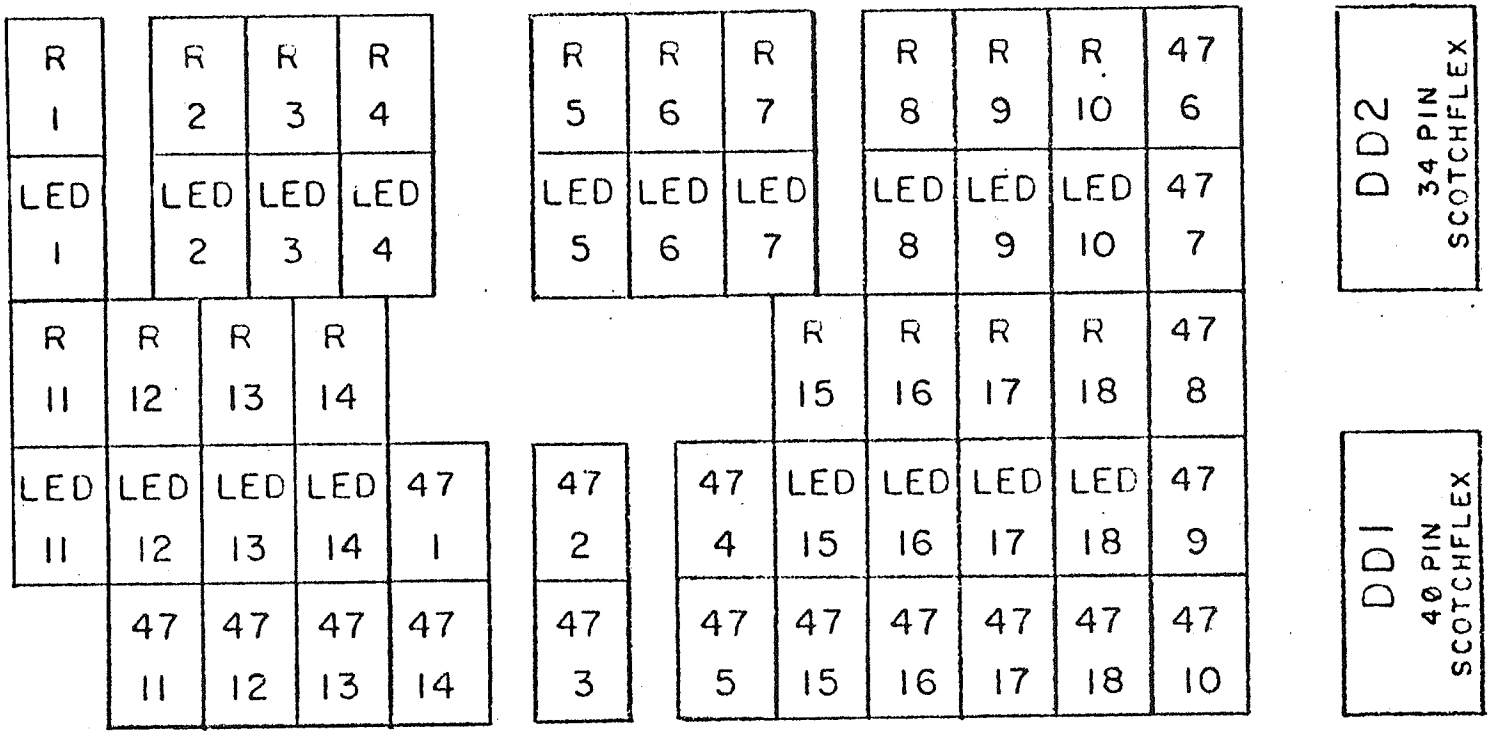


Figure A-13: Pulse Height Detector Controller (Device 6) (Board D8)

TOP VIEW



R = 100 Ω RESISTOR BLOCK
LED = 7 SEGMENT LED DISPLAY
47 = SN74LS47

Figure A-14(a): Carrier Frequency, Pulse Repitition Frequency and Pulse Width (Cycles)

Display Board Layout

	PIN NO			74LS74 POSITION	DIGIT	
DGND	18	1	+5V			
B	19	2	A	11	3	PULSE REPITITION FREQUENCY
D	20	3	C			
B	21	4	A	12	2	
D	22	5	C			
B	23	6	A	13	1	
D	24	7	C			
B	25	8	A	14	0	
D	26	9	C			
B	27	10	A	15	3	PULSE WIDTH (CYCLES)
D	28	11	C			
B	29	12	A	16	2	
D	30	13	C			
B	31	14	A	17	1	
D	32	15	C			
B	33	16	A	18	0	
D	34	17	C			

* 34 pin scotchflex connector

Figure A-14(b): Connector DD2 Pin Specifications

	PIN NO.			74LS74 POSITION	DIGIT
B	2	1	A	1	9
D	4	3	C		
B	6	5	A	2	8
D	8	7	C		
B	10	9	A	3	7
D	12	11	C		
B	14	13	A	4	6
D	16	15	C		
B	18	17	A	5	5
D	20	19	C		
B	22	21	A	6	4
D	24	23	C		
B	26	25	A	7	3
D	28	27	C		
B	30	29	A	8	2
D	32	31	C		
B	34	33	A	9	2
D	36	35	C		
B	38	37	A	10	0
D	40	39	C		

CARRIER FREQUENCY

* 40 pin scotchflex connector

Figure A-14(c): Connector DD1 Pin Specifications

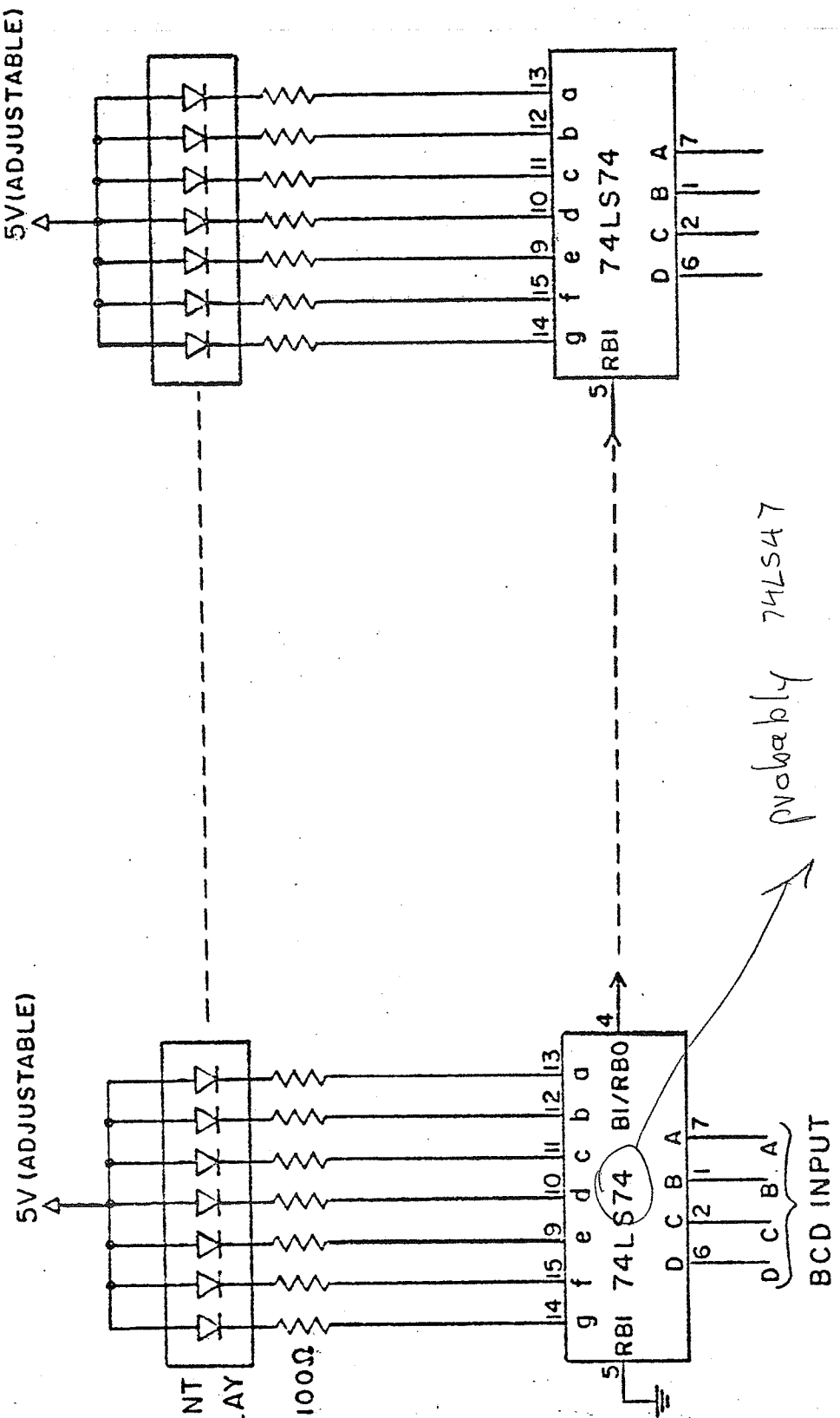


Figure A-15: BCD to 7-segment Decoder Chain Circuit for Carrier Frequency, Pulse Repitition Frequency and Pulse Width (Cycles) Display Board

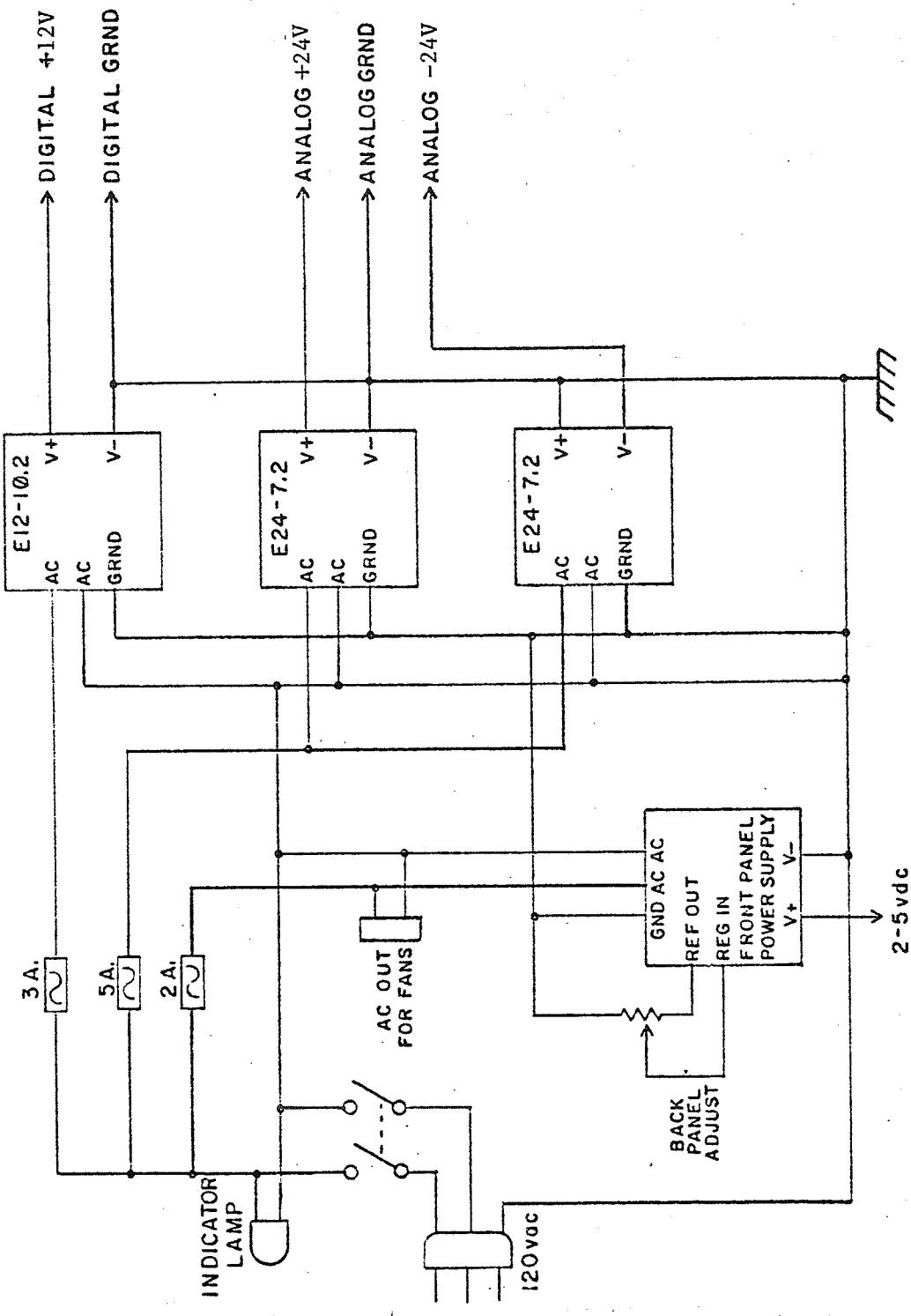


Figure A-16: Power Supply for the Circuits

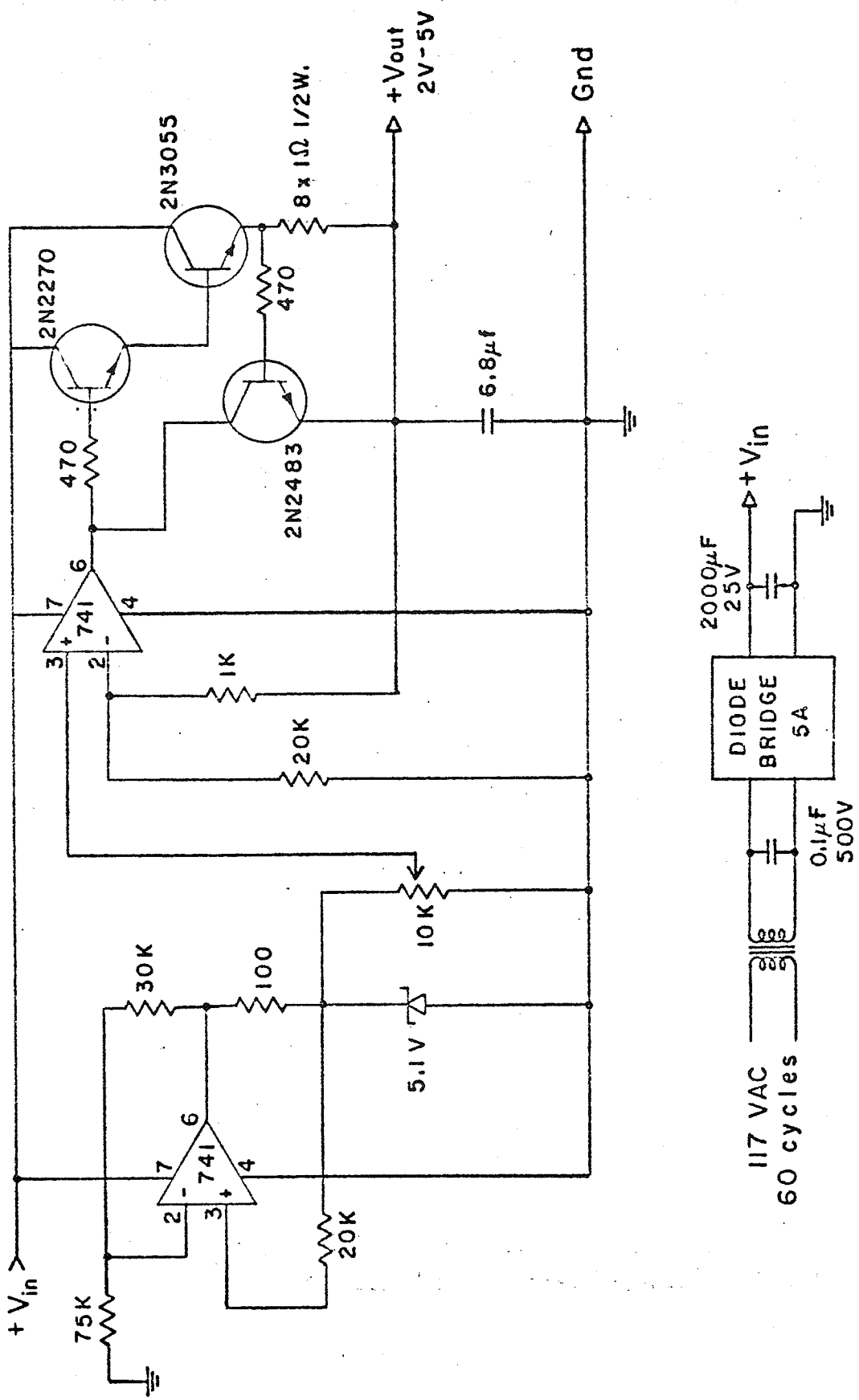


Figure A-17: Power Supply for the Front Panel Displays

Appendix B

Suggested Vendors of Integrated Circuits

Part Number	Description	Vendor
AM 500	100 MHz bandwidth operational amplifier	Datel
Am 685	ECL voltage comparator	Advanced Micro Devices
Am 687	ECL dual voltage comparator	Advanced Micro Devices
DG 190AP	2-channel high-speed driver with SPDT junction FET switches	Siliconix
DG 381CJ	Dual SPST CMOS analog switch	Siliconix
LH 0063CK	100 MHz bandwidth buffer amplifier	National
LM 318	Operational amplifier	National
MC 10125	ECL to TTL translator	Motorola
1435	1 GHz bandwidth operational amplifier	Teledyne Philbrick
μA 740	FET input operational amplifier	Fairchild

Appendix C

List of Symbols

SYMBOLS	DESCRIPTION
1. ABUF	Buffer register of the programmable attenuator controller.
2. ADC	Analog-to-digital converter.
3. CLIPBUF	Buffer register of the clipper controller.
4. CLIPCSR	Control status register of the clipper controller.
5. DAC	Digital-to-analog converter.
6. DBUF	Digit buffer register of the HP 8660B synthesizer controller.
7. DCSR	Control status register of the HP 8660B synthesizer controller.
8. DIO	Digital input/output part of the Perkin Elmer 7/32 computer.
9. DISBUF	Display buffer register of the HP 8660B synthesizer controller, controls strobing of latched BCD digits to carrier frequency display on system front panel.
10. DOPDA	Delayed OPDA, this signal is a 1 μs pulse triggered by the falling edge of OPDA.
11. FTB-BUF	Buffer register of the HP 5328A Universal Counter controller for programming function and time base.
12. OPDA	Output data available, hand-shake signal from the DIO.
13. PAMP-BUF	Buffer register of the programmable gain amplifier controller.
14. PHD-CSR	Control status register of the pulse height detector controller.
15. RECORDER-BUF-(A,B or C)	Recorder output buffer registers of the HP 5328A Universal Counter controller.
16. RECORDER-CSR	Control status register of the HP 5328A Universal Counter controller, recorder status control.
17. WBUF	Buffer register of the programmable window generator controller.

SYMBOLS	DESCRIPTION
18. WCSR	Control status register of the programmable window generator controller.
19. 041A-BUF	Buffer register of the HP 5328A Universal Counter controller for programming Channel A of the 041 input section.
20. 041B-BUF	Buffer register of the HP 5328A Universal lounter controller for programming Channel B of the 041 input section.
21. 041-CSR	Control status register of the HP 5328A Universal Counter controller, 041 input section status control.
22.	Perkin Elmer 7/32 mimicouputer.