A DATA ACQUISITION SYSTEM FOR ULTRASONIC TOMOGRAPHY

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Summary

Living tissues can be characterized by their interaction with ultrasound. Our research involves measuring the frequency dependent amplitude and time-of-flight of ultrasound after it passes through biological materials. This information is processed to produce tomographic images of the material being studied. This type of tomographic images yields resolutions of 0.5 cm in the low MHz ultrasonic frequency range. This paper describes the data acquisition circuitry used in these computerized tomography systems. A block diagram of the system is given in Figure 1.

System Description

All the image reconstruction tasks and experiment controls are handled by an Interdata 7/32 computer and all communications of the system to the Interdata 7/32 are performed by an analog-to-digital (A/D) input channel and two digital input/output ports (DIO). A device controller is responsible for interfacing the different system data acquisition electronics to the Interdata 7/32.

The ultrasound signal transmitted is either a single broadband pulse or a discrete frequency tone burst. The signal source is an HP 8660B sine wave synthesizer (output frequency range: 0.01 - 110 MHz) whose frequency and amplitude are programmable and controlled by the 7/32. In order to free the zero crossing detection circuit, which is the frontend of the programmable window generator, from the constraints of the low signal amplitude, the signal amplitude of the HP 8660B is set constant at maximum. The synthesizer output drives a high speed FET input buffer amplifier. The buffer amplifier drives a programmable attenuator and a programmable window generator. The programmable attenuator varies the signal output of the buffer amplifier in 64 steps and has a dynamic range of 36 dB. The programmable window generator utilizes high speed Schottky TTL logic chips which have minimal gate delays to produce a window coherent with the signal zero crossings. This window generator has a capability of producing a window whose width is equivalent to 0.5, 1, 2, 4, 8, 16, 32, 64, or 128 cycles of the signal. The window signal and the programmable attenuator output are mixed by the double balanced mixer (DBM) and a pulse of appropriate pulse width and amplitude is thus produced. The signal is then amplified by a power amplifier which in turn excites the transmit transducer and transmits an ultrasound signal through the tissue under test. In order to measure the time-of-flight of the ultrasound signal, averaging of many signals must be done. An HP 5328A Universal Counter is used for this, and the resolution obtained depends on the number of intervals averaged. A 2 nanosecond resolution is desirable in some measurements and requires averaging of 100 intervals. The HP 5328A Universal Counter is started by triggering its channel A input by a rising edge generated by the clipper. The clipper is actually a signal detection circuit which generates a rising edge to trigger channel A of the counter when any signal occurs at the double balanced mixer output.

After the signal passes through the tissue under test, it is detected by an ultrasonic transducer and amplified by the HP 461A amplifier. The amplified signal causes the clipper circuit to generate another rising edge to trigger channel B of the HP 5328A counter and thus stopping the counter after the appropriate number of intervals, thus yielding time-of-flight data. When discrete frequency tone bursts are transmitted, the HP 461A drives a programmable filter with selectable cut-offs to reduce noise. The filtered signal is then further amplified by a four stage programmable gain amplifier to condition the signal to an appropriate amplitude range of the pulse height detector. The pulse height detector produces a DC level output proportional to the peak, rectified signal amplitude. This DC level is then digitized by an analog-to-digital converter in the Interdata 7/32 through an A/D input channel.

The programmable filter and the pulse height detector are bypassed for a broadband pulse. The signal output of the HP 461A is amplified by the programmable amplifier and goes through a buffer amplifier to the TRW 8-BIT video analog-to-digital converter (TDC 1007J) which has a sampling rate of 30 MHz. A high speed parallel memory buffer must be used to buffer all the data points. A parallel memory system is used to obtain a high data transfer rate. Thus by sequential clocking of several blocks of slower memories, a higher bandwidth is achieved to match the 30 MHz sampling rate. This memory buffer empties its contents to the Interdata 7/32 through DIO 2. Appropriate signal processing such as Fourier analysis can then be performed.
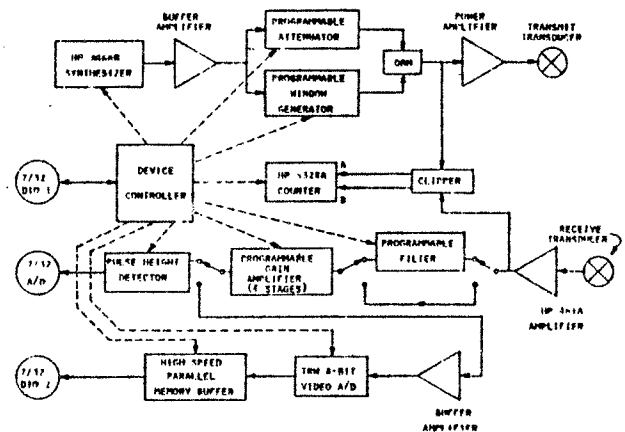
Acknowledgement

Figure 1. System Block Diagram.